FIG . 1

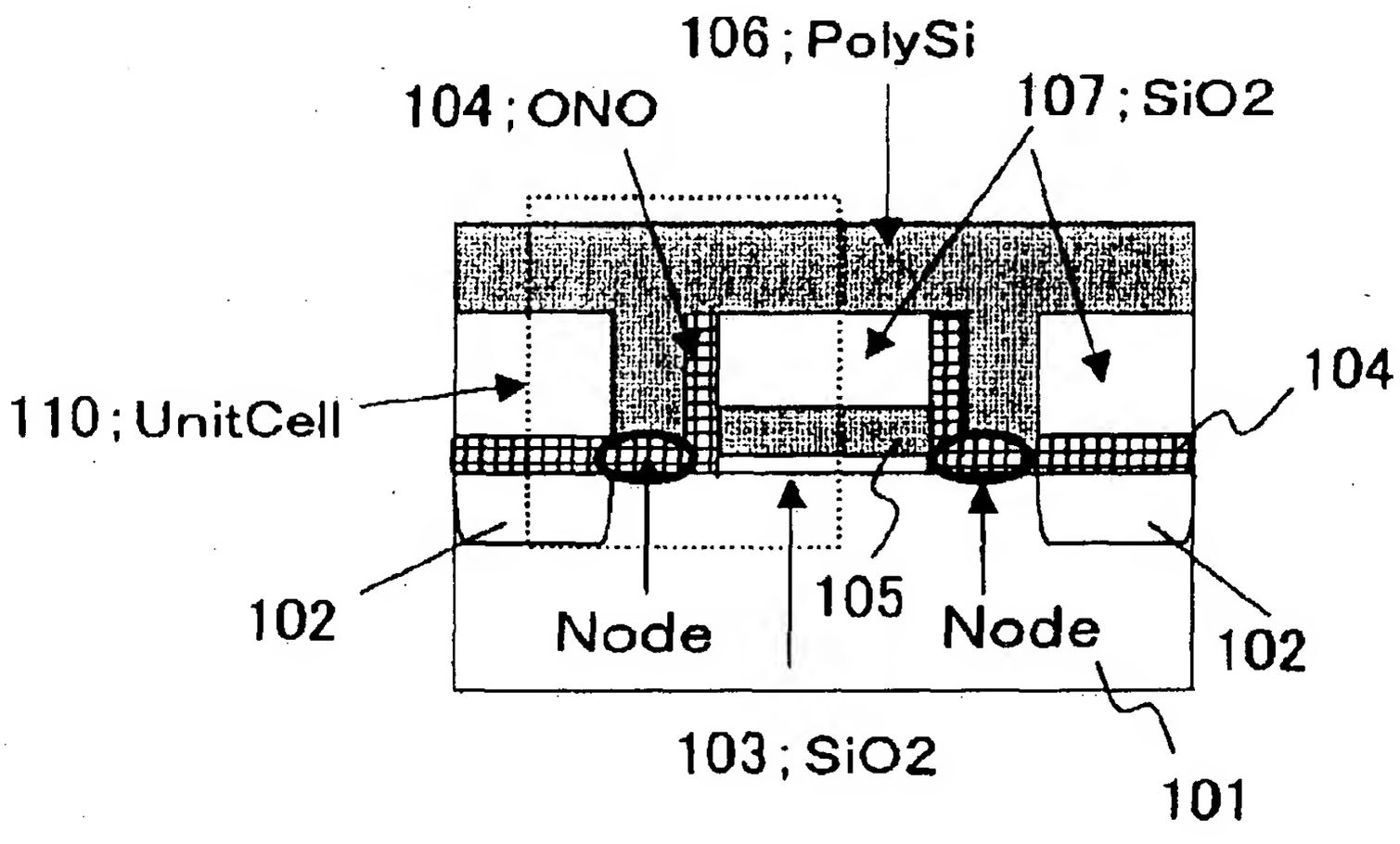

106 ; PolySi
104 ; ONO
107 ; SiO2
110 ; UnitCell
104
102
Node
105
Node
102
103 ; SiO2
101

FIG . 2

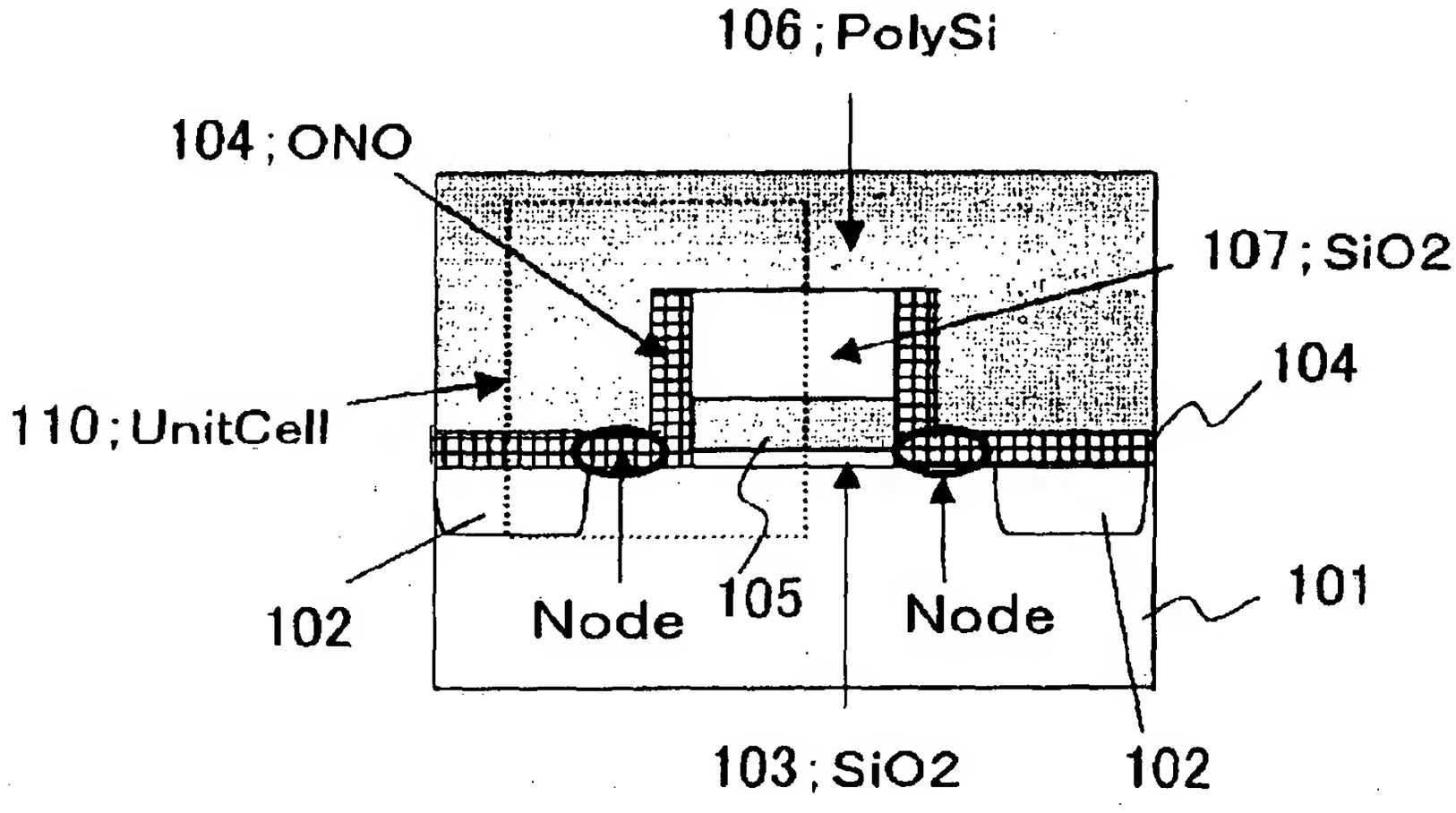

106 ; PolySi
104 ; ONO
107 ; SiO2
104
110 ; UnitCell
101
102
Node
105
Node
103 ; SiO2
102

FIG . 3A

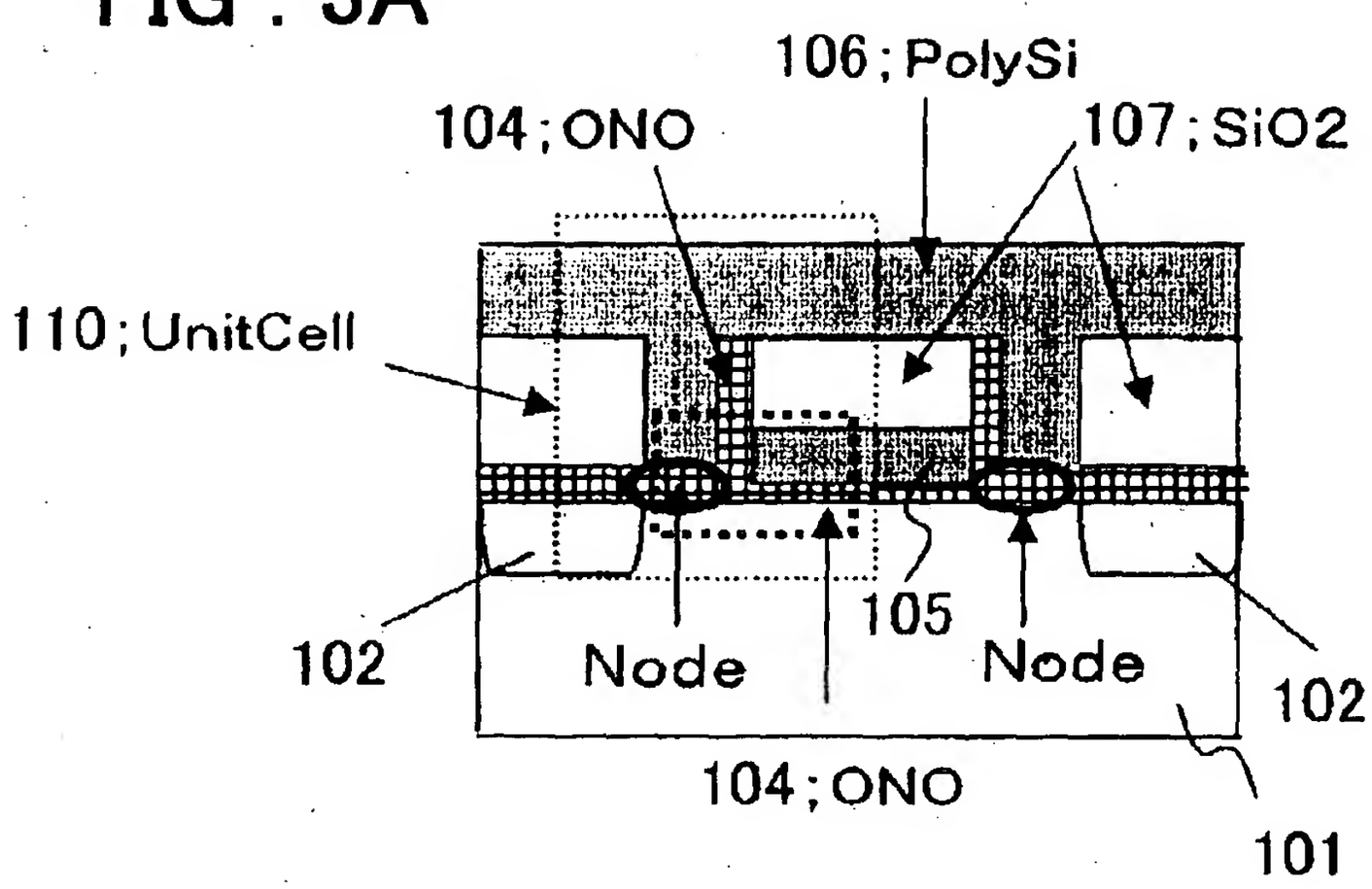
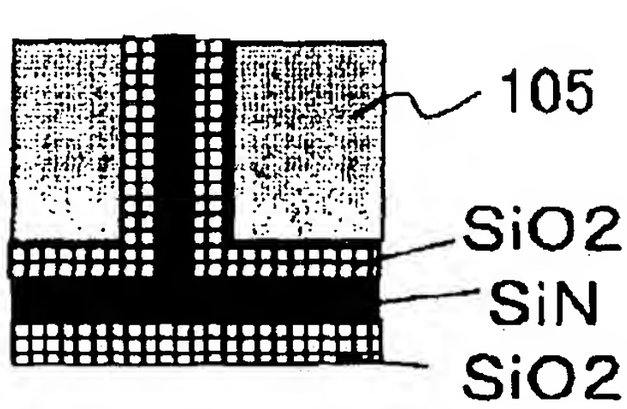


FIG . 3B



ONO STRUCTURE

FIG . 4

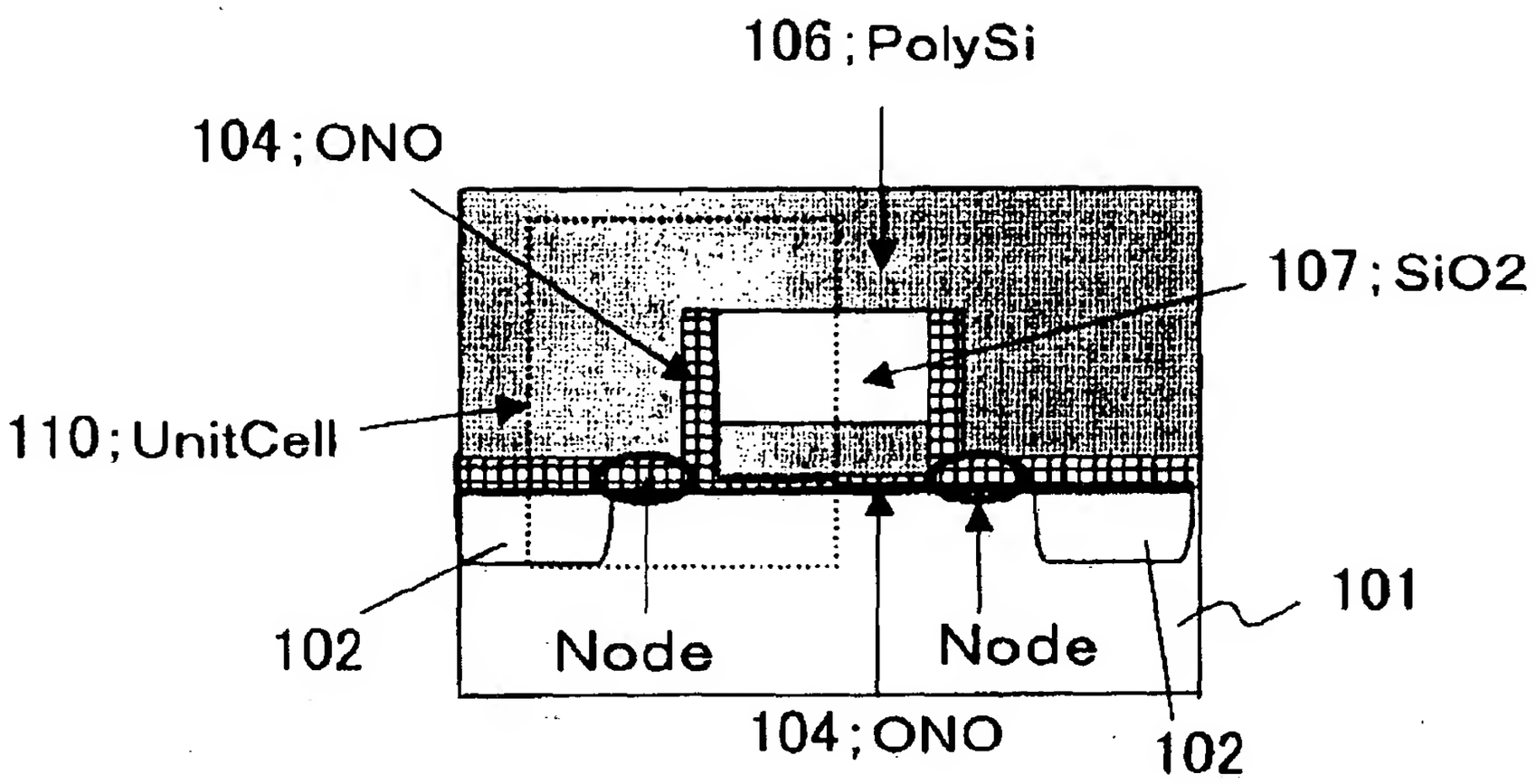

106 ; PolySi
104 ; ONO
107 ; SiO2
110 ; UnitCell
102
Node
Node
101
104 ; ONO
102

FIG . 5A

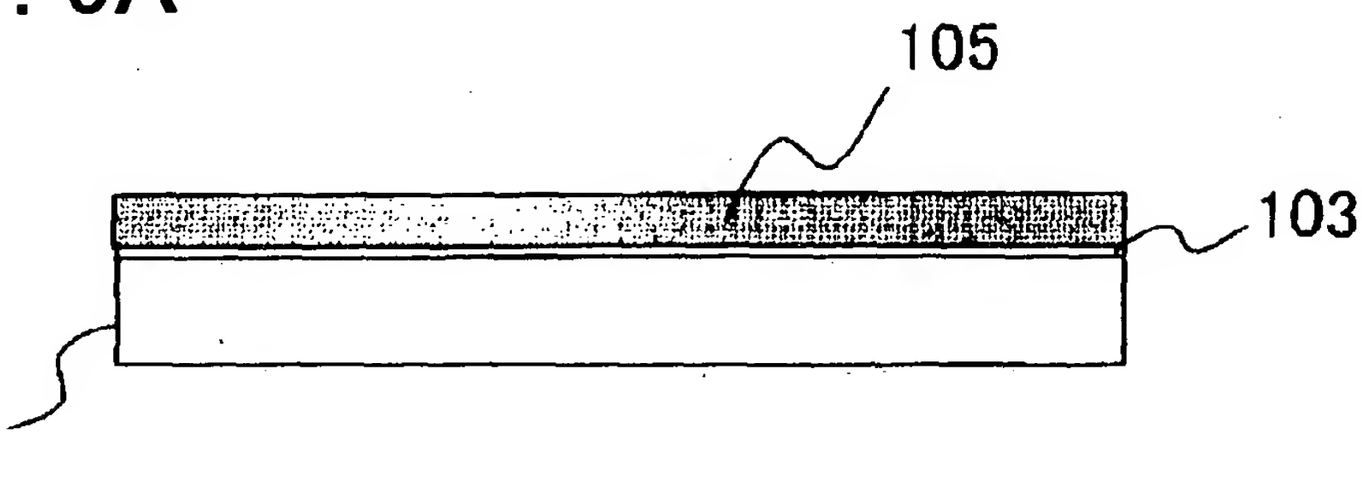


FIG . 5B

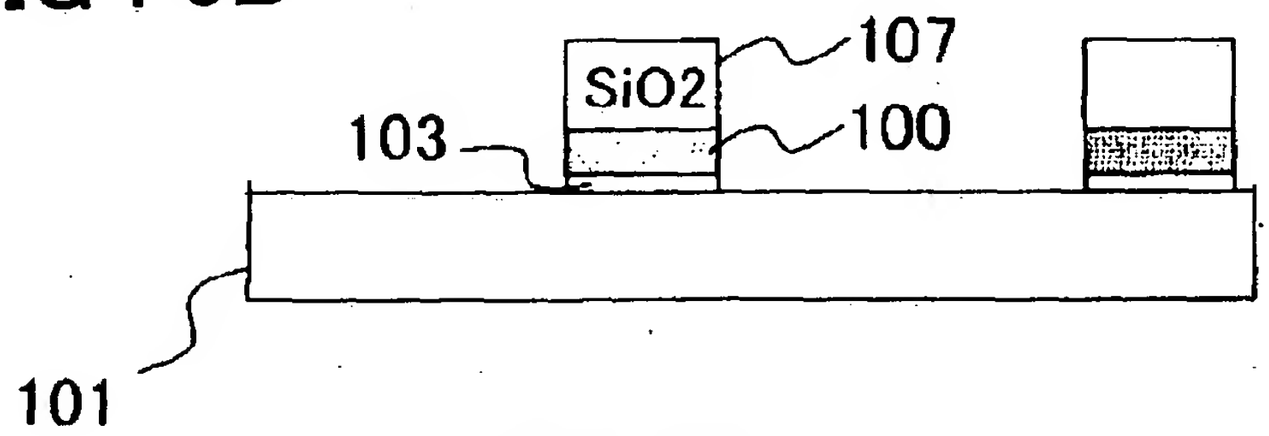


FIG . 5C

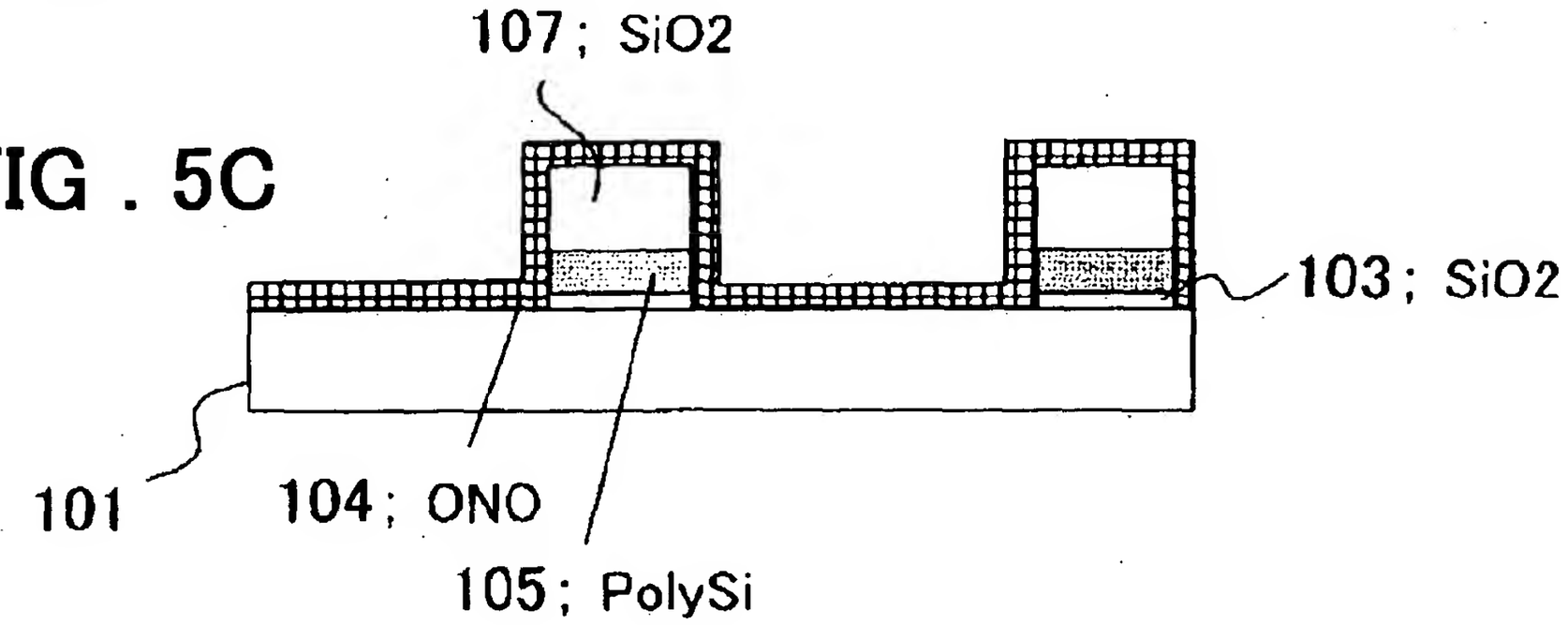


FIG . 6A

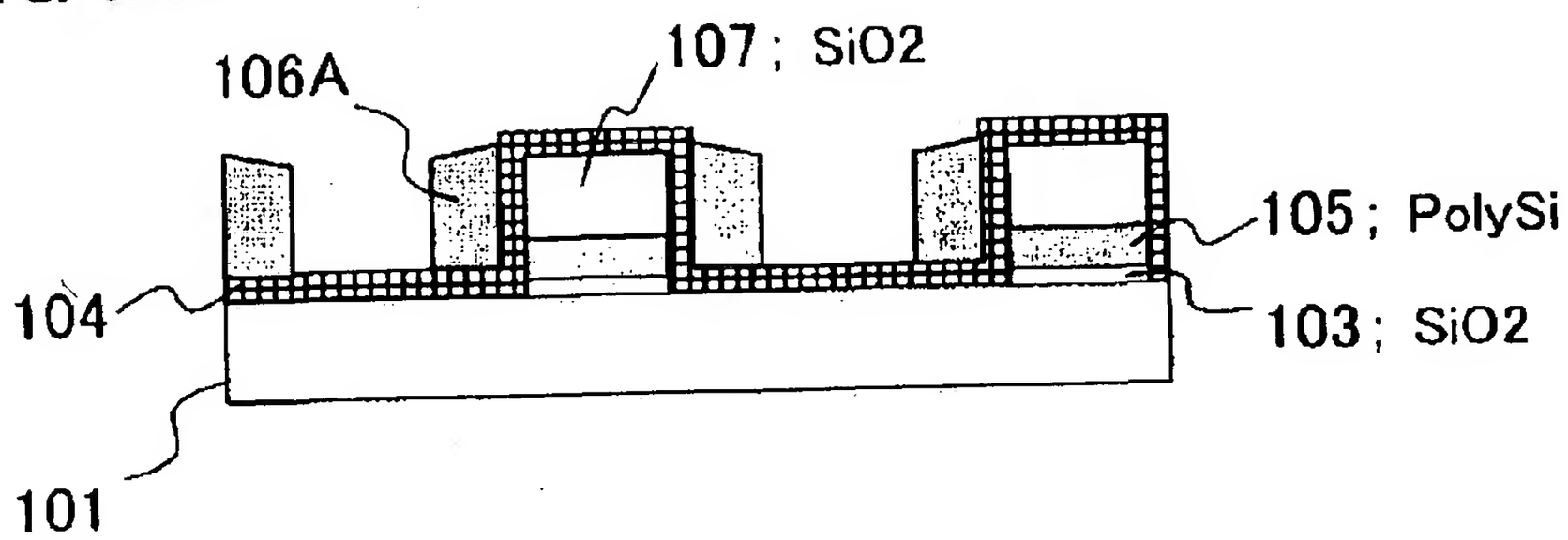

106A
107 ; SiO2
105 ; PolySi
104
103 ; SiO2
101

FIG . 6B

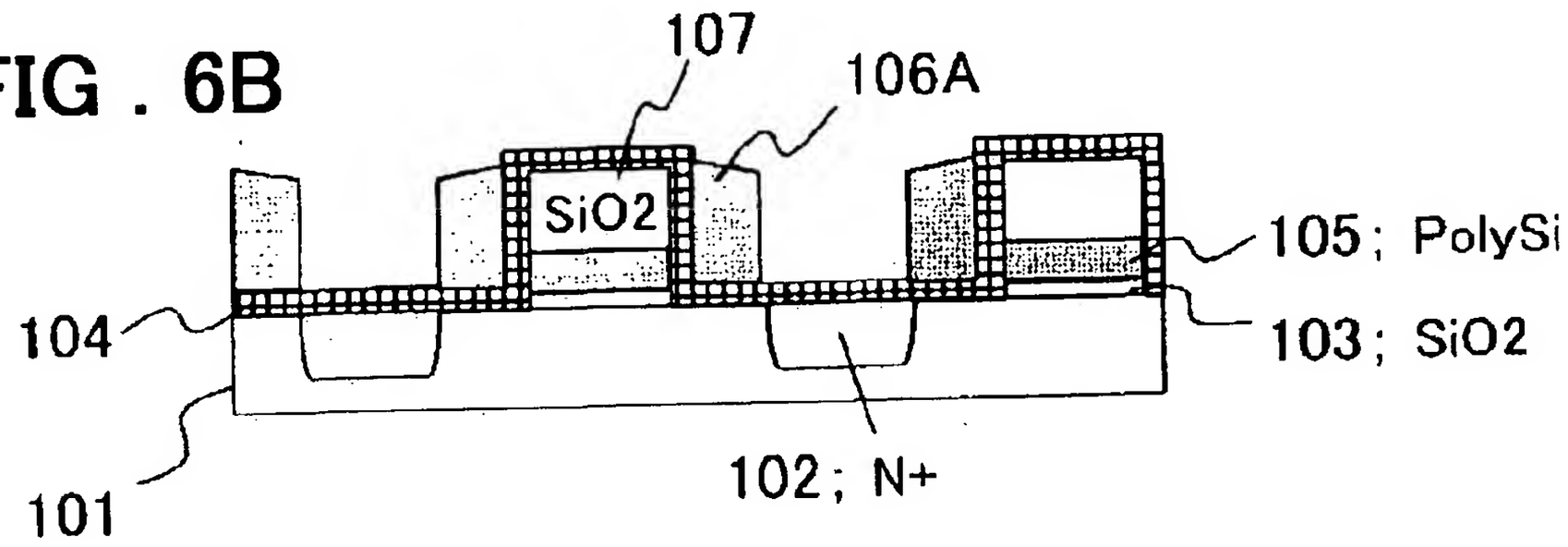

107
106A
SiO2
105 ; PolySi
104
103 ; SiO2
101
102 ; N+

FIG . 7A

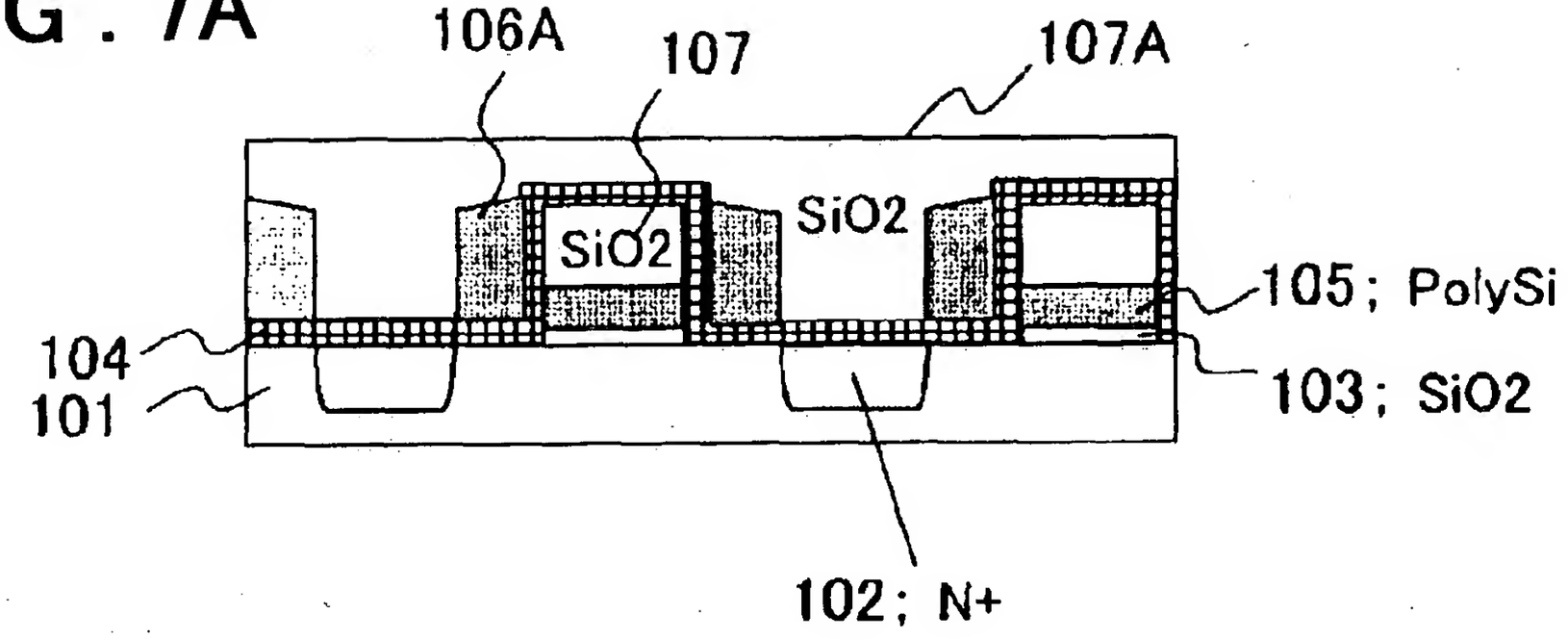
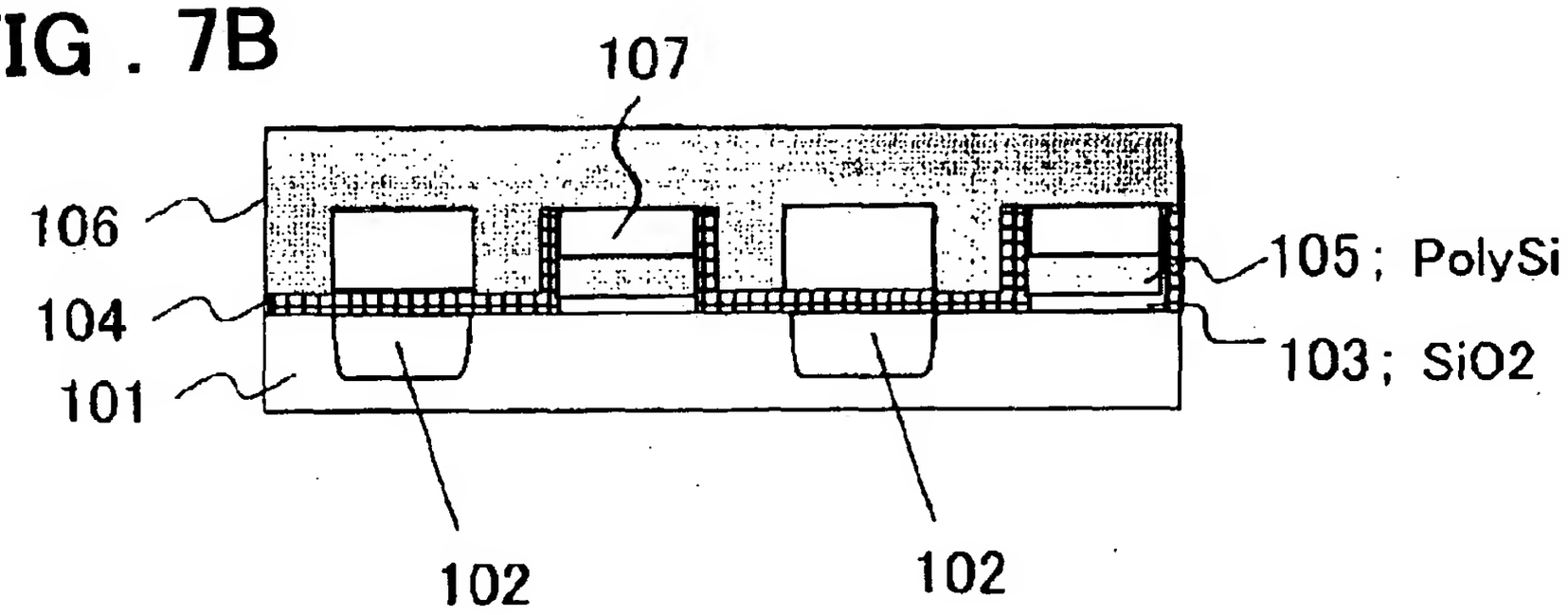

106A
107
107A
SiO2
SiO2
105; PolySi
104
101
103; SiO2
102; N+

FIG . 7B


107
106
104
101
105; PolySi
103; SiO2
102
102

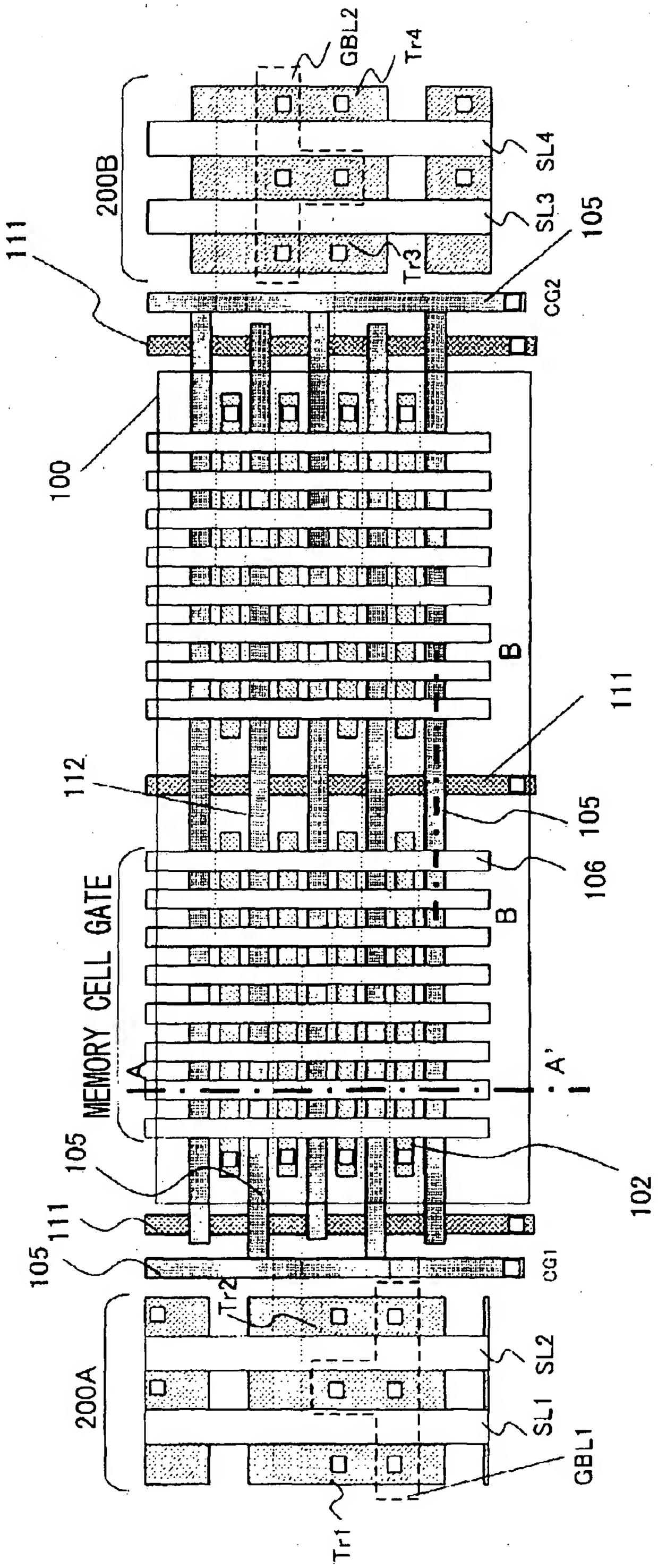

GBL2
Tr4
200B
SL4
SL3
105
111
Tr3
CG2
100
112
B
111
106
105
MEMORY CELL GATE
A
A'
105
102
111
105
Tr2
CG1
200A
SL2
SL1
GBL1
Tr1

FIG. 8

FIG . 9A

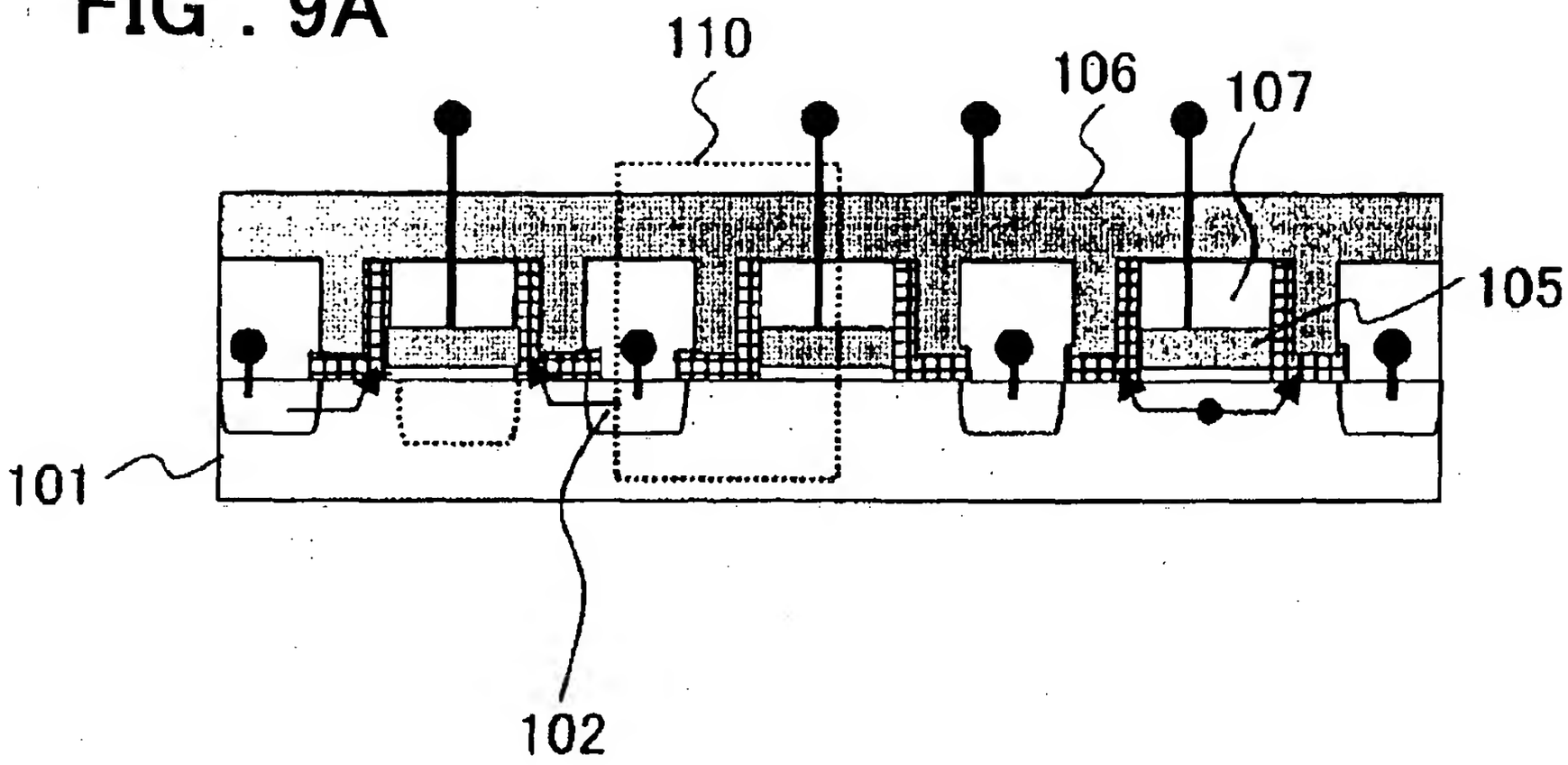
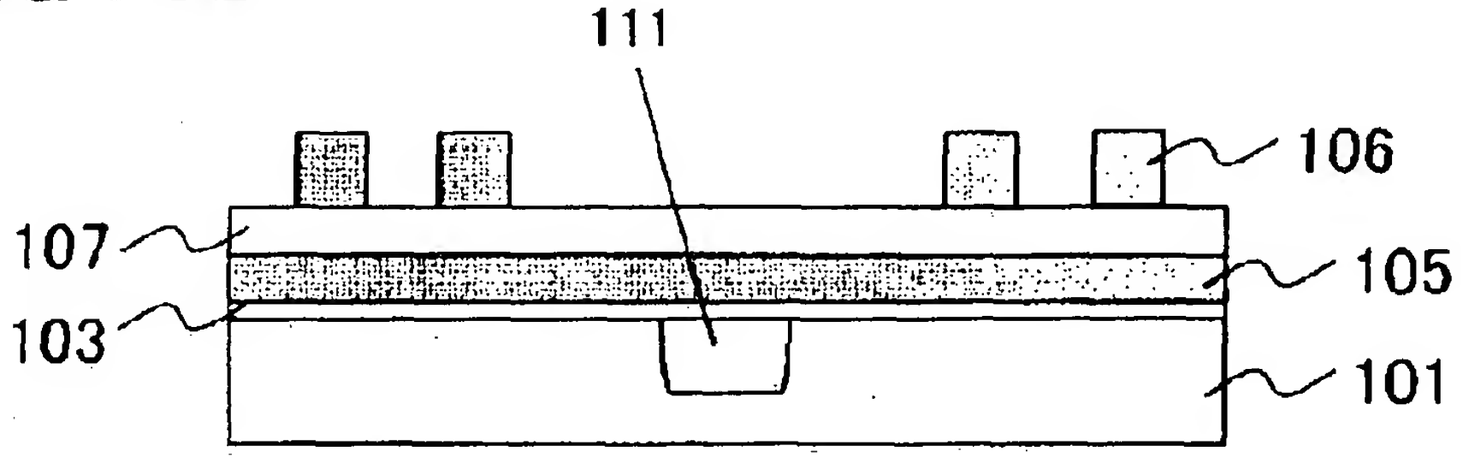


FIG . 9B



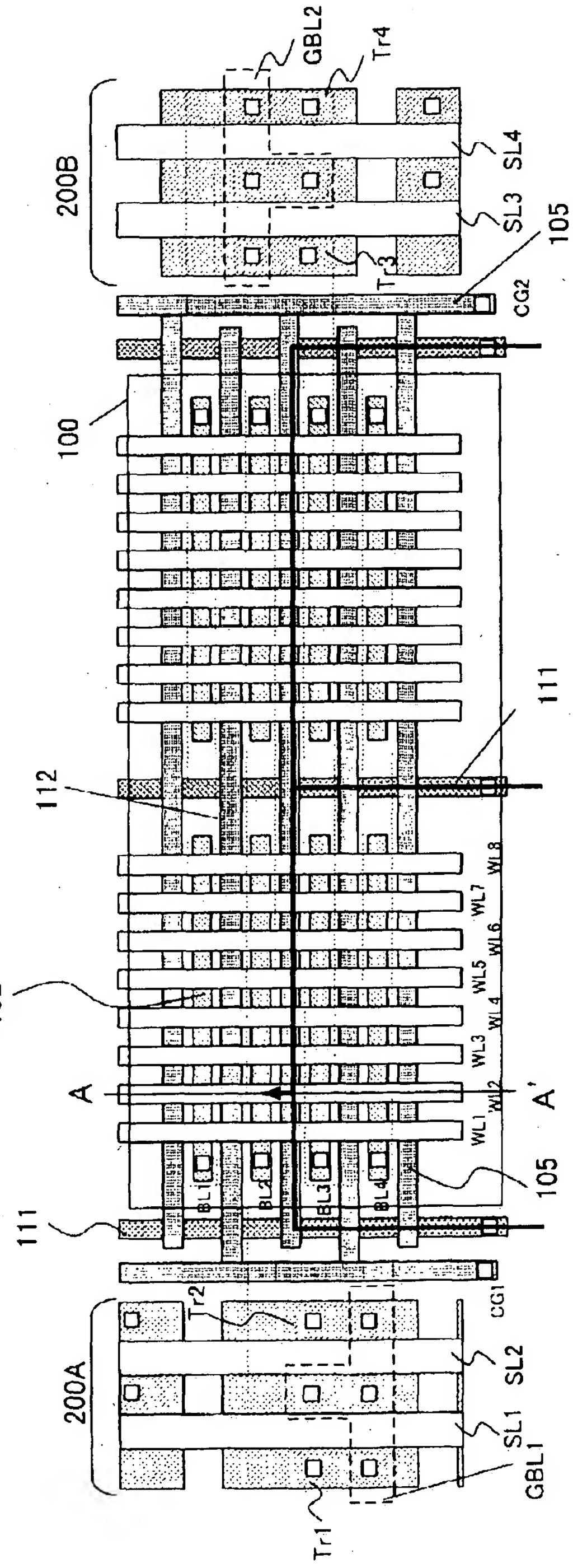
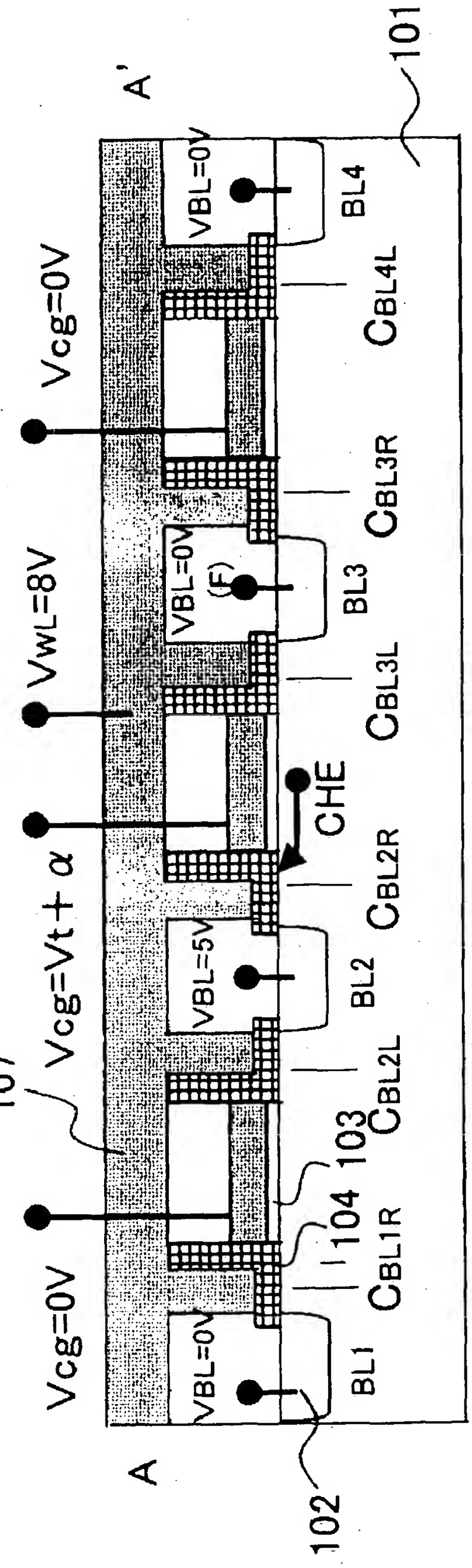

GBL2
Tr4
200B
SL4
SL3
105
Tr3
CG2
100
111
112
102
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
A
A'
BL1
BL2
BL3
BL4
105
111
CG1
Tr2
200A
SL2
SL1
GBL1
Tr1

FIG. 10

FIG . 11


A
A'
101
102
103
104
107
Vcg=0V
Vcg=Vt+α
VWL=8V
VBL=0V
VBL=5V
(F)
CHE
BL1
BL2
BL3
BL4
CBL1R
CBL2L
CBL2R
CBL3L
CBL3R
CBL4L

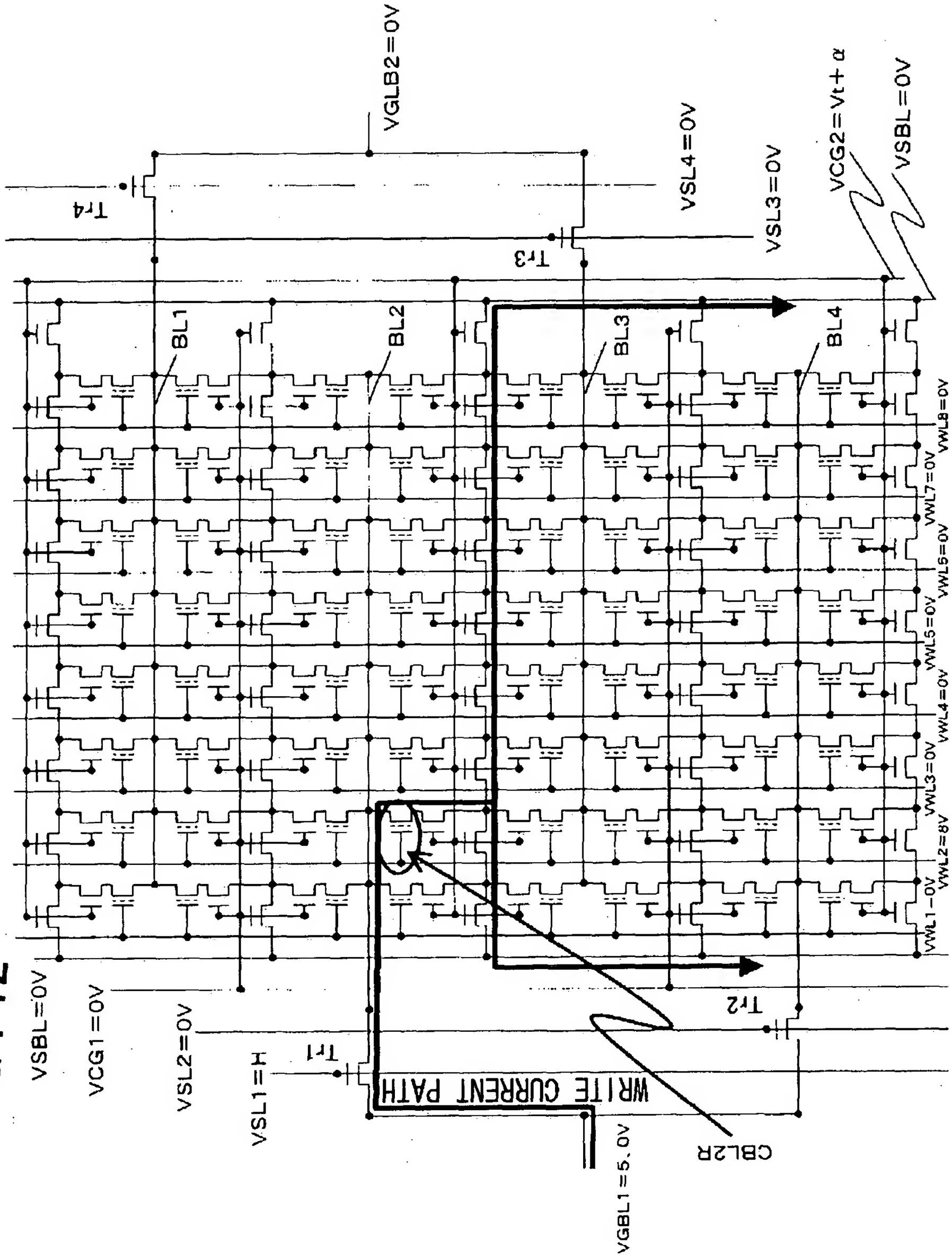

VGLB2=0V
VSL4=0V
VSL3=0V
VCG2=Vt+α
VSBL=0V
Tr4
Tr3
BL1
BL2
BL3
BL4
VWL8=0V
VWL7=0V
VWL6=0V
VWL5=0V
VWL4=0V
VWL3=0V
VWL2=8V
VWL1=0V
VSBL=0V
VCG1=0V
VSL2=0V
VSL1=H
Tr1
Tr2
WRITE CURRENT PATH
CBL2R
VGBL1=5.0V

FIG. 12

FIG . 13A

L SIDE Prog

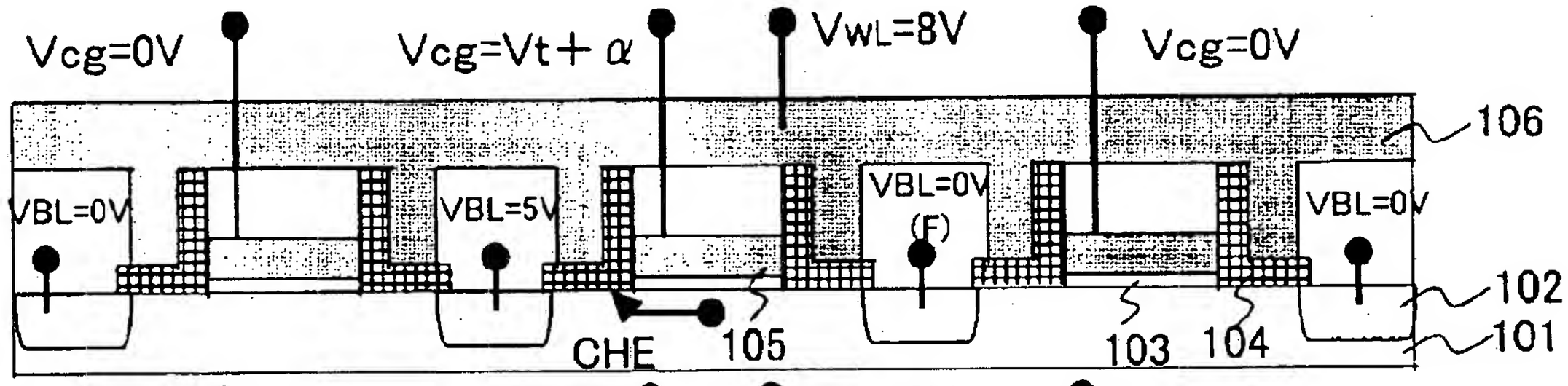


FIG . 13B

R SIDE Prog

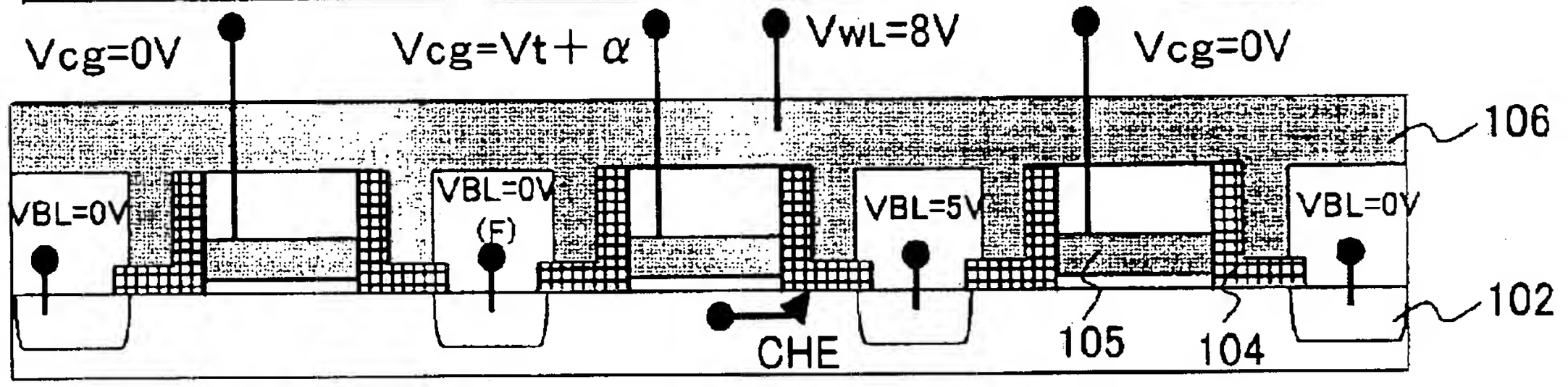


FIG . 13C

BOTH SIDEProg

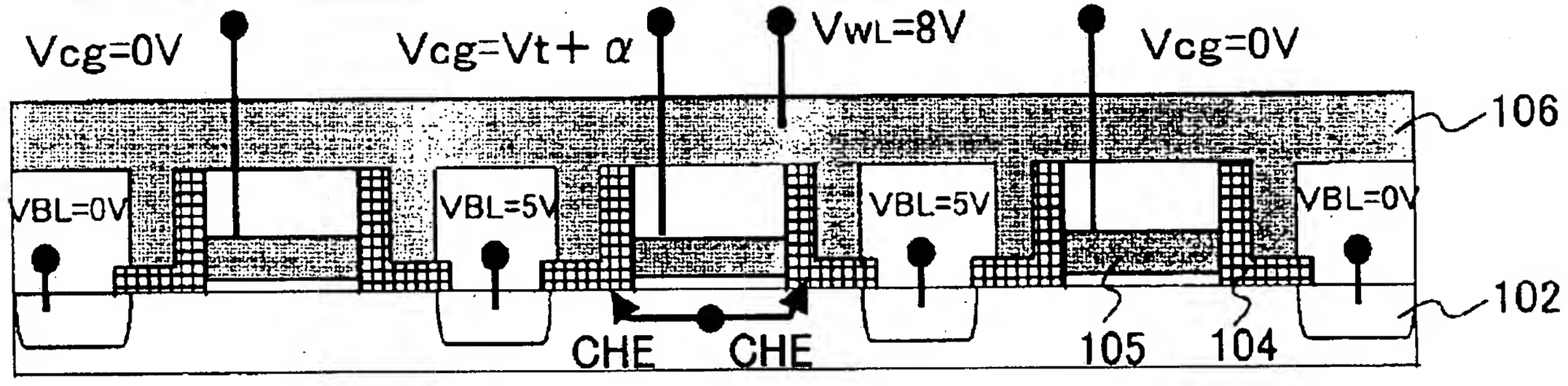


FIG .14

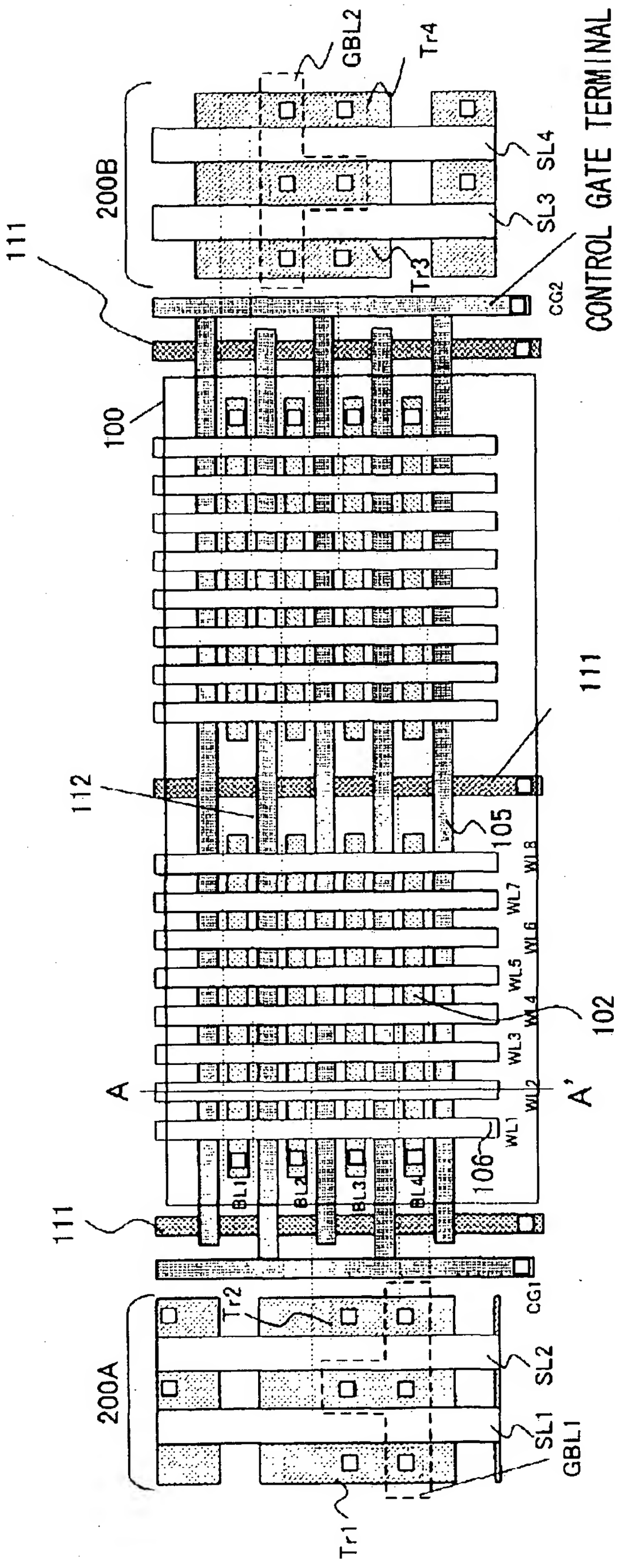
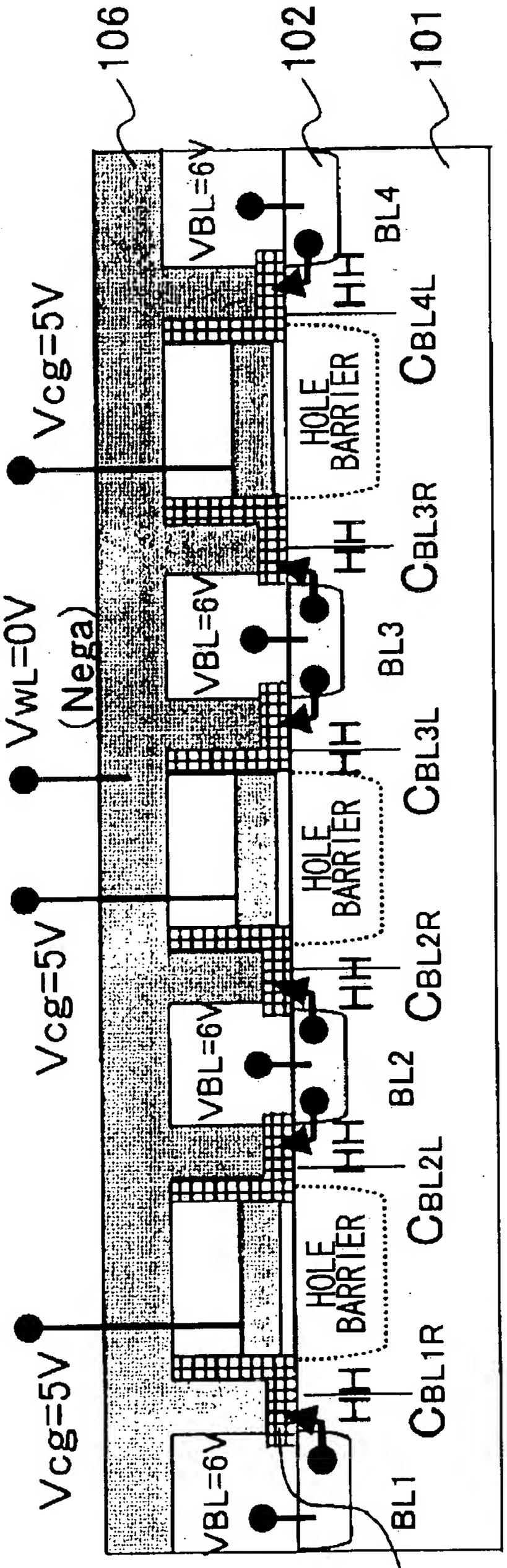

GBL2
Tr4
200B
111
SL4
SL3
Tr3
CG2
CONTROL GATE TERMINAL
100
112
105
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
102
A
A'
BL1
BL2
BL3
BL4
106
Tr2
CG1
200A
SL2
SL1
GBL1
Tr1

FIG .15


106
102
101
VBL=6V
BL4
HH
CBL4L
HOLE BARRIER
Vcg=5V
VWL=0V
(Nega)
Vcg=5V
VBL=6V
BL3
HH
CBL3R
HOLE BARRIER
HH
CBL3L
VBL=6V
BL2
HH
CBL2R
HOLE BARRIER
HH
CBL2L
Vcg=5V
VBL=6V
BL1
HH
CBL1R
104

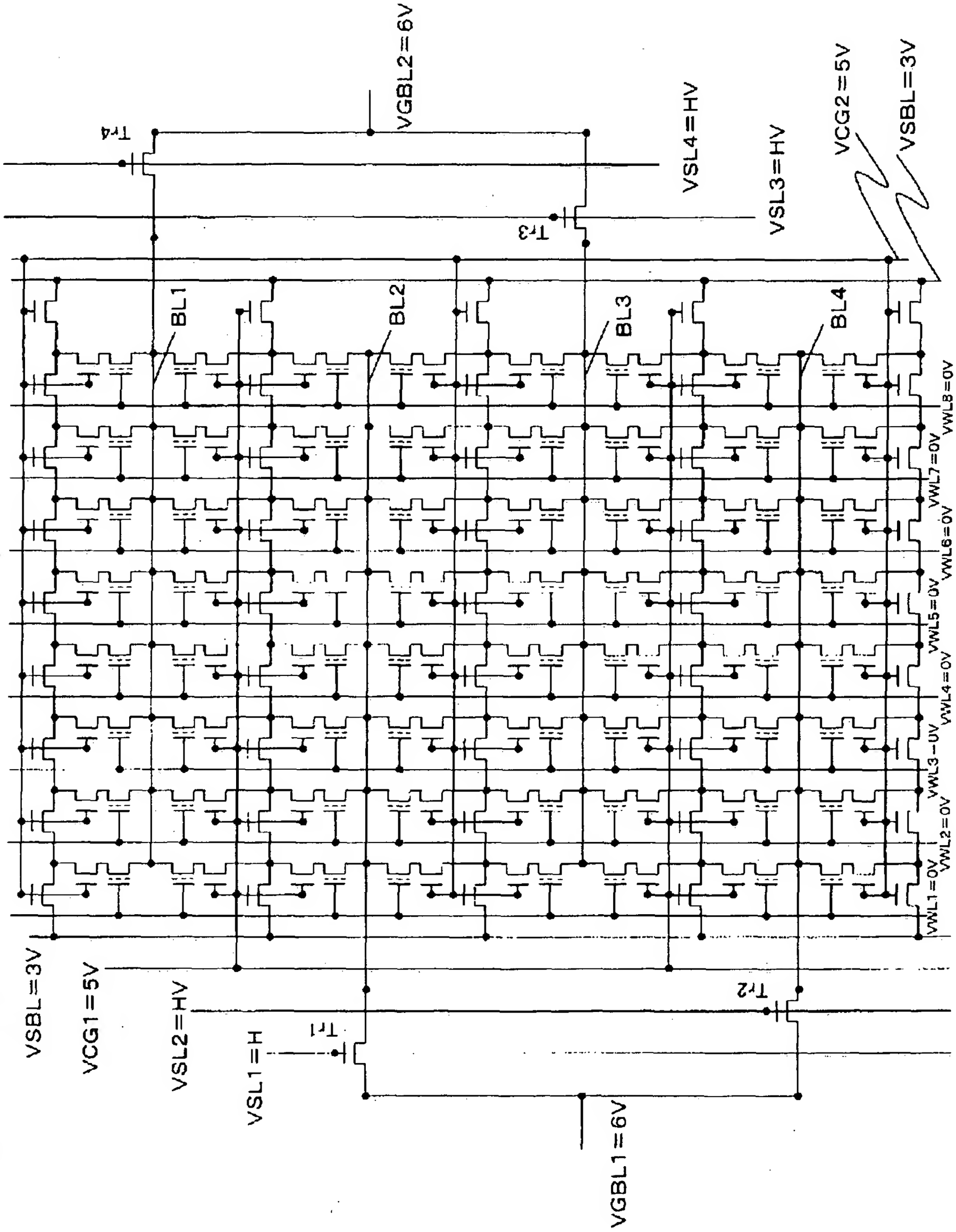

VGBL2=6V
VSL4=HV
VSL3=HV
VCG2=5V
VSBL=3V
Tr4
Tr3
BL1
BL2
BL3
BL4
VWL8=0V
VWL7=0V
VWL6=0V
VWL5=0V
VWL4=0V
VWL3=0V
VWL2=0V
VWL1=0V
VSBL=3V
VCG1=5V
VSL2=HV
VSL1=H
Tr1
Tr2
VGBL1=6V

FIG . 16

FIG . 17A

After Prog

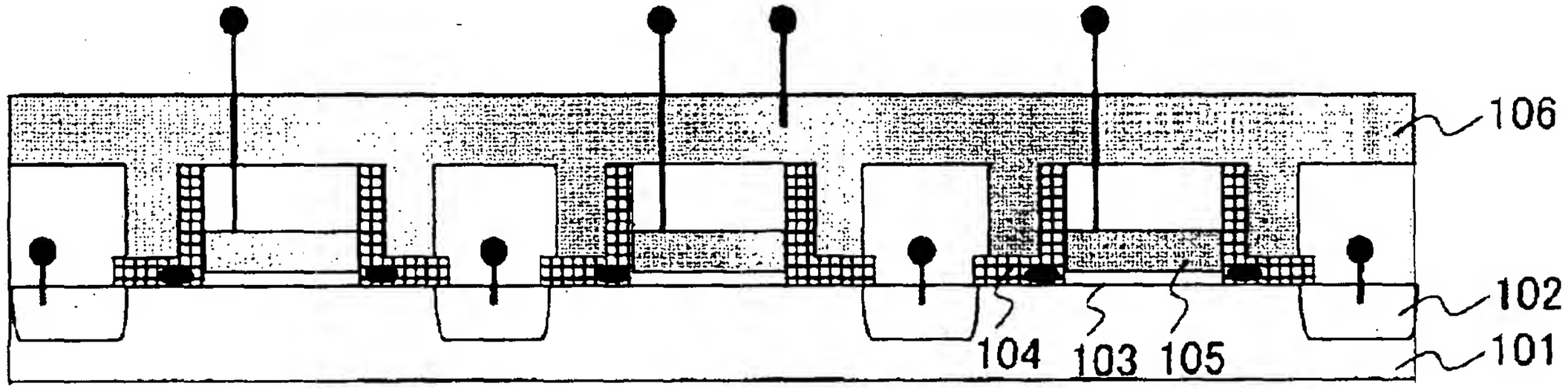


FIG . 17B

Pre Prog

Lsid ／Rside
INDEPENDENT Program

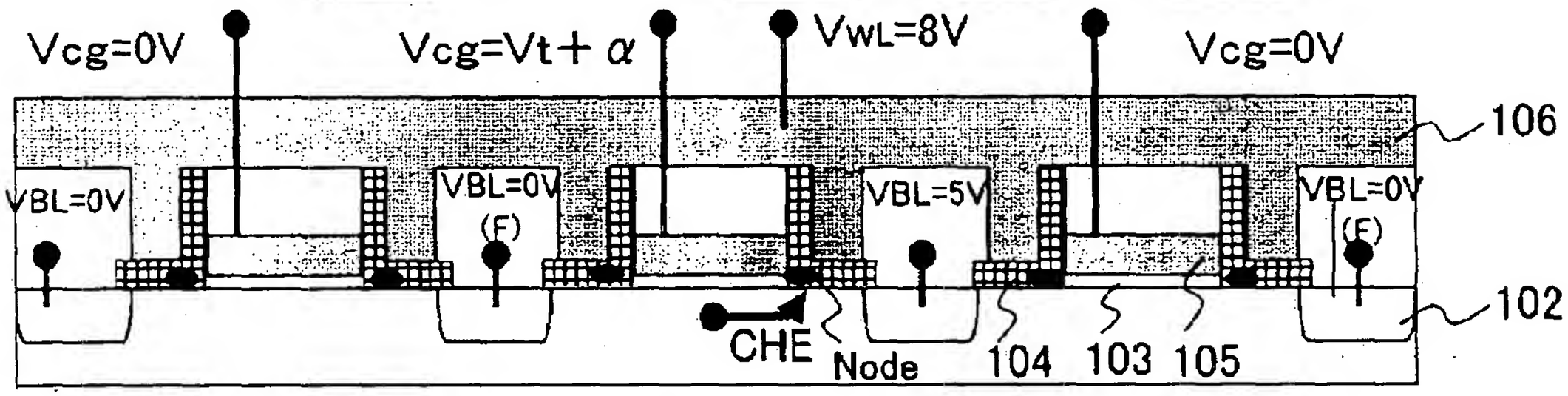
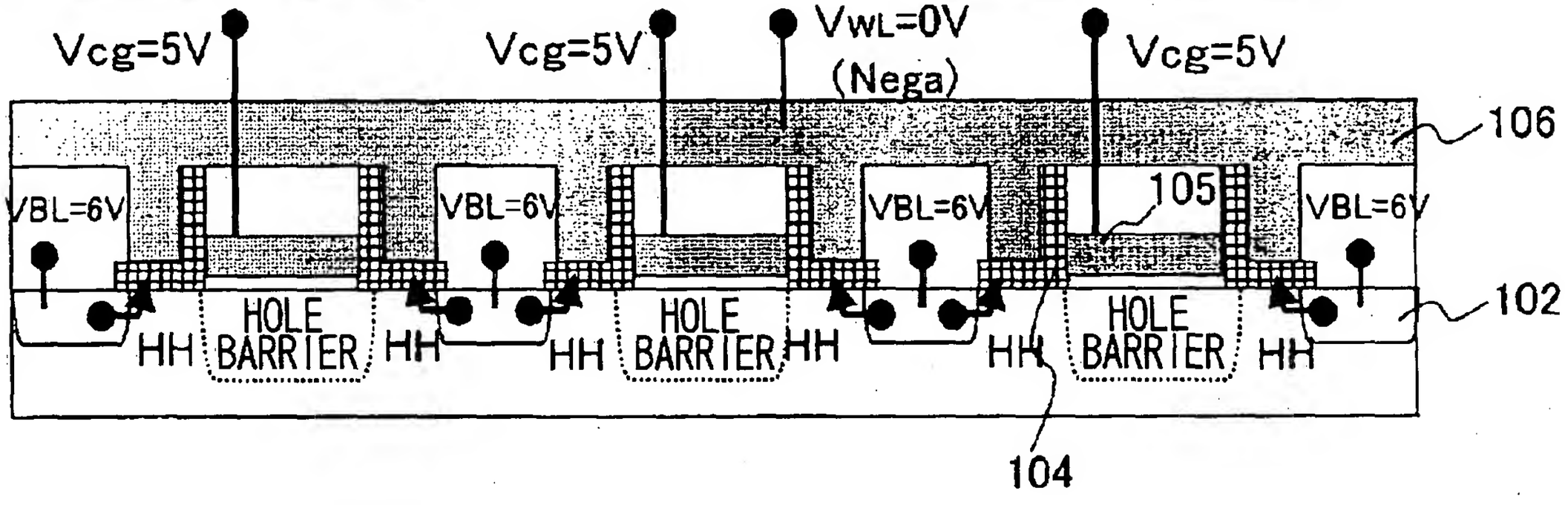


FIG . 17C

Erase

FLASH ERASE



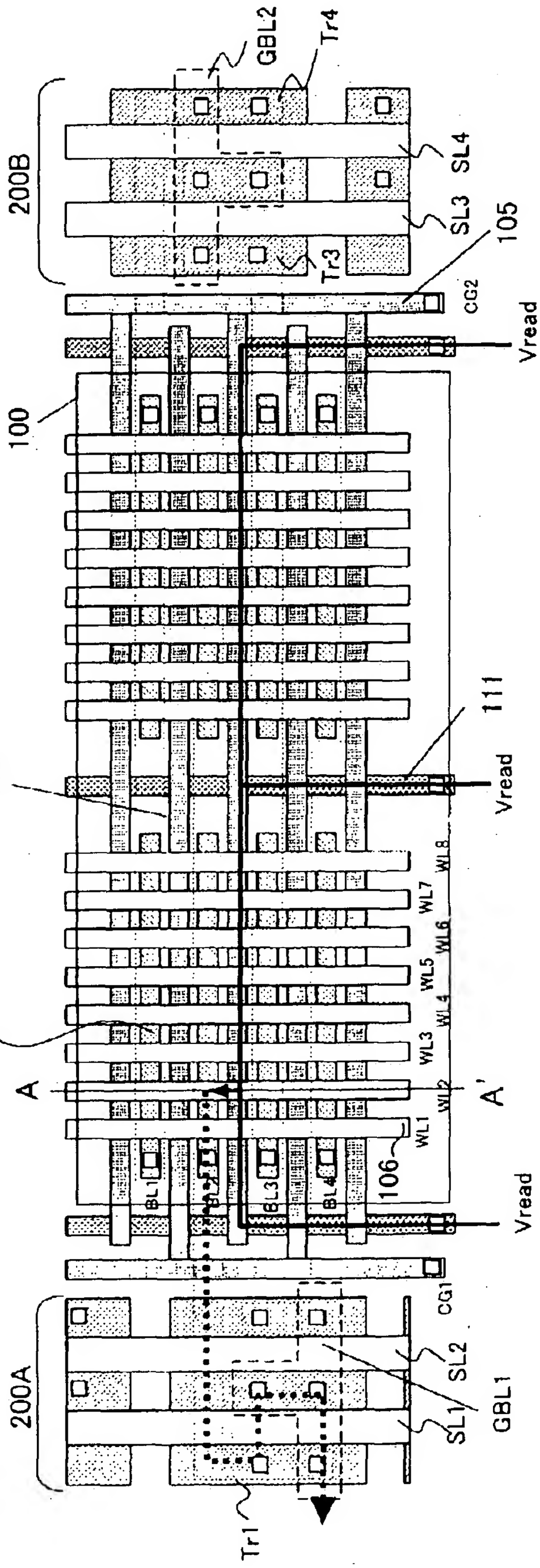

GBL2
Tr4
200B
SL4
SL3
105
Tr3
CG2
Vread
100
112
111
Vread
102
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
A
A'
106
BL1
BL2
BL3
BL4
Vread
CG1
200A
SL2
SL1
GBL1
Tr1

FIG. 18

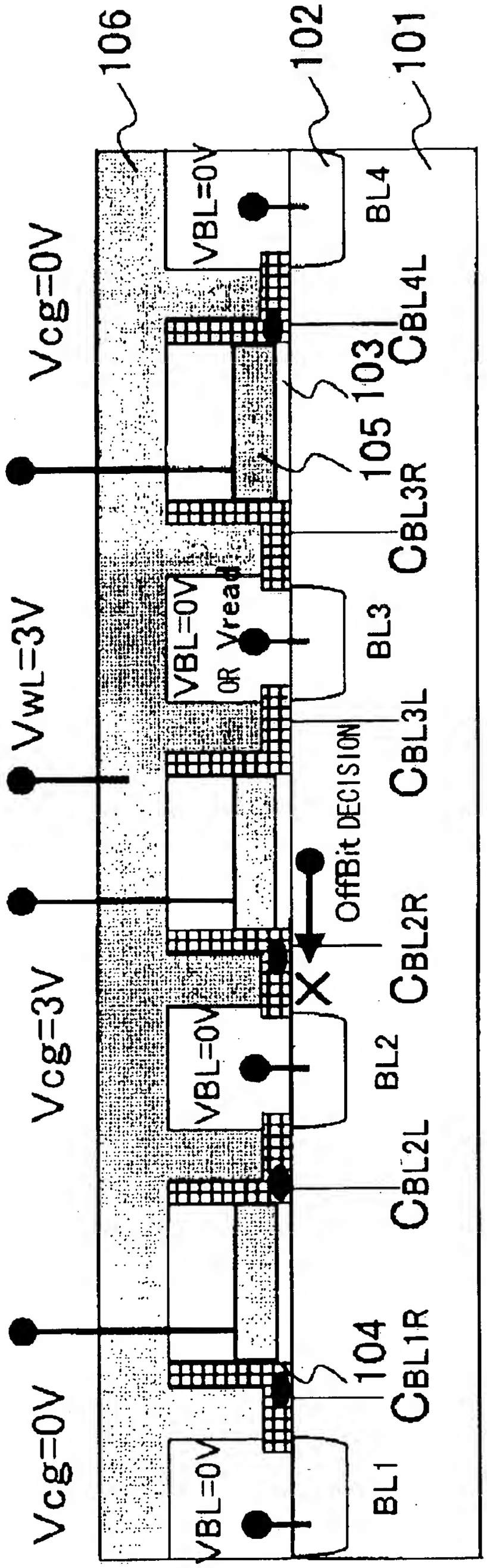

106
102
101
Vcg=0V
VBL=0V
BL4
CBL4L
103
105
CBL3R
VWL=3V
VBL=0V
OR Vread
BL3
CBL3L
OffBit DECISION
Vcg=3V
X
BL2
CBL2R
CBL2L
104
Vcg=0V
VBL=0V
BL1
CBL1R

FIG. 19

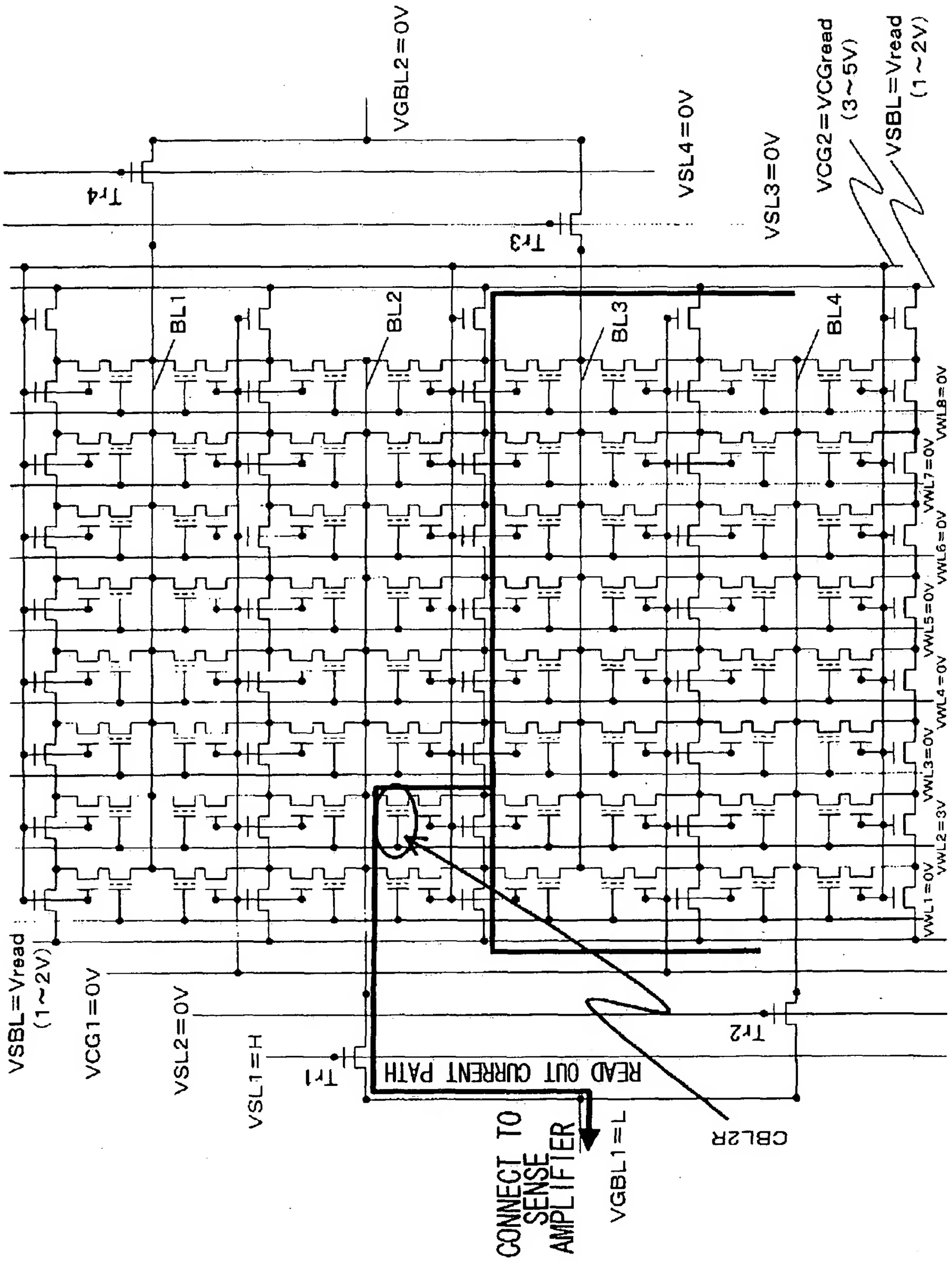

VGBL2=0V
VSL4=0V
VSL3=0V
VCG2=VCGread
(3~5V)
VSBL=Vread
(1~2V)
Tr4
Tr3
BL1
BL2
BL3
BL4
VWL8=0V
VWL7=0V
VWL6=0V
VWL5=0V
VWL4=0V
VWL3=0V
VWL2=3V
VWL1=0V
VSBL=Vread
(1~2V)
VCG1=0V
VSL2=0V
VSL1=H
Tr1
Tr2
READ OUT CURRENT PATH
CBL2R
CONNECT TO SENSE AMPLIFIER
VGBL1=L

FIG. 20

FIG . 21A

Lbit Read

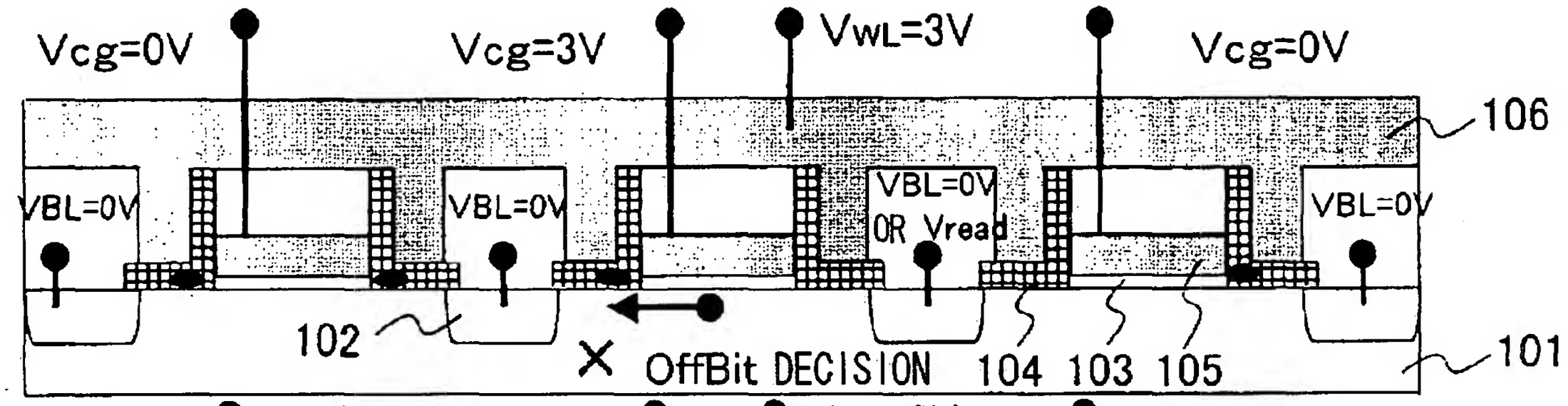


FIG . 21B

Rbit Read

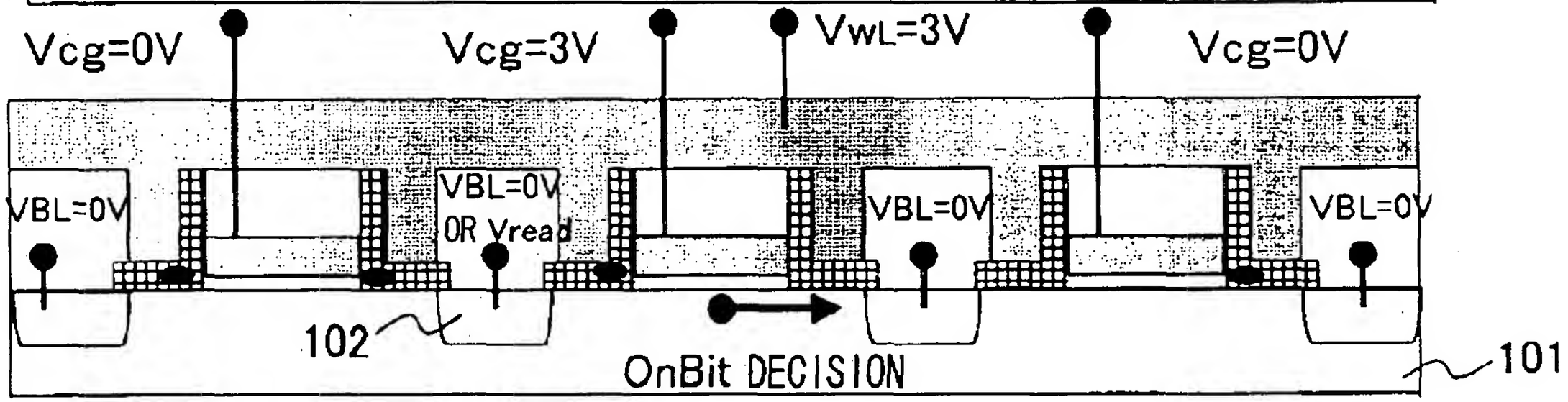


FIG . 21C

Lbit Read

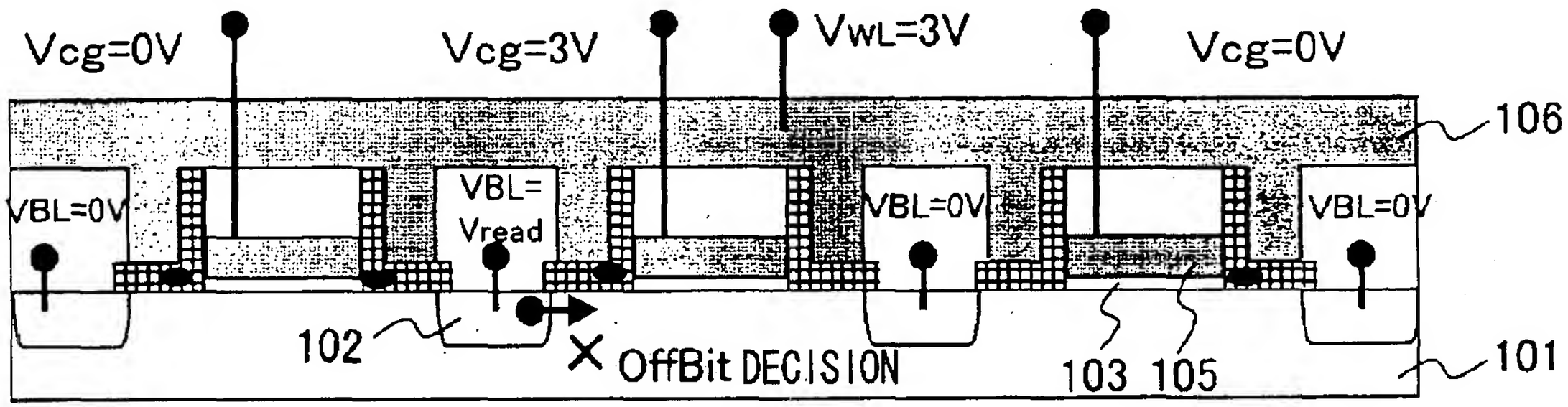


FIG . 22

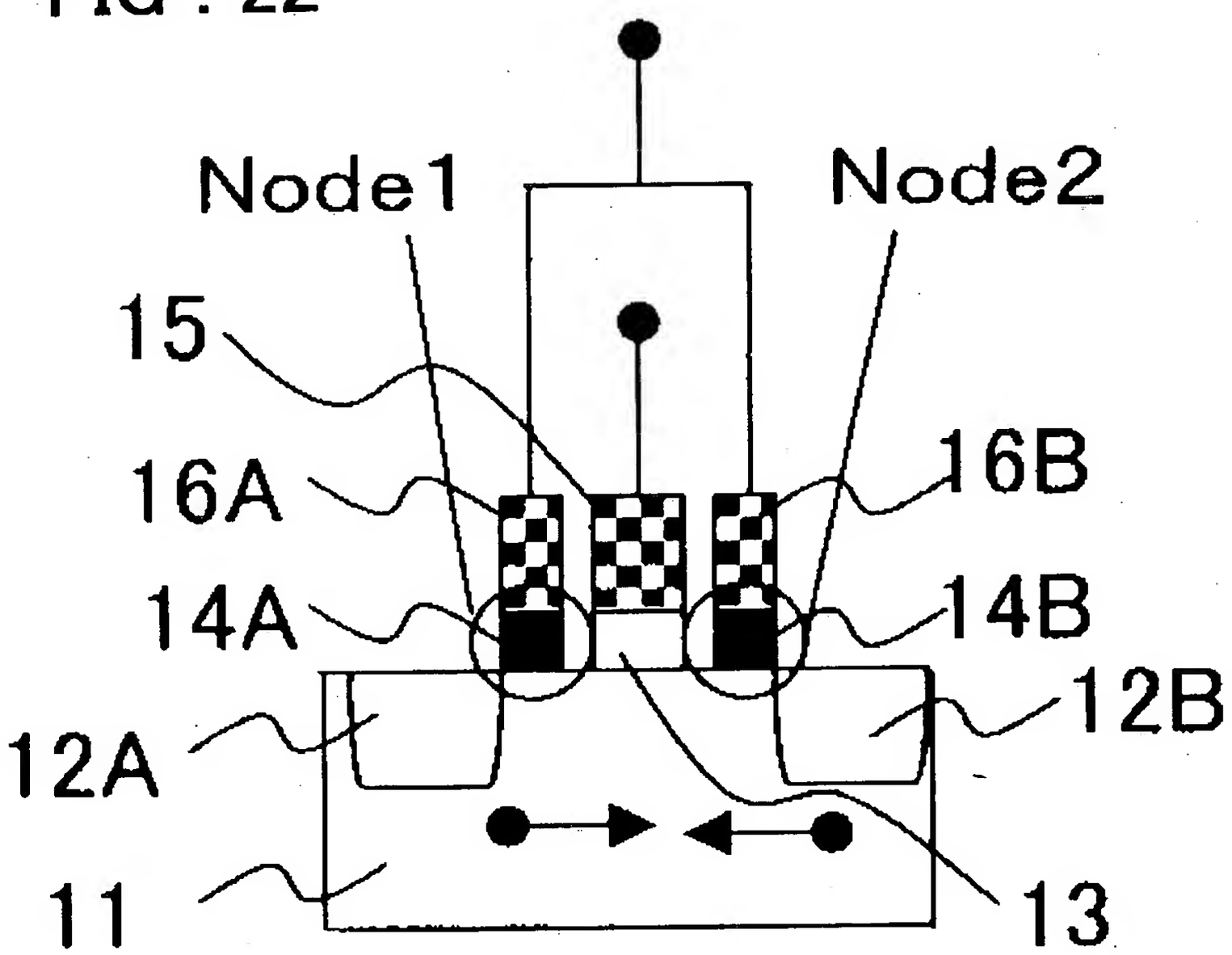


FIG . 23 PRIOR ART

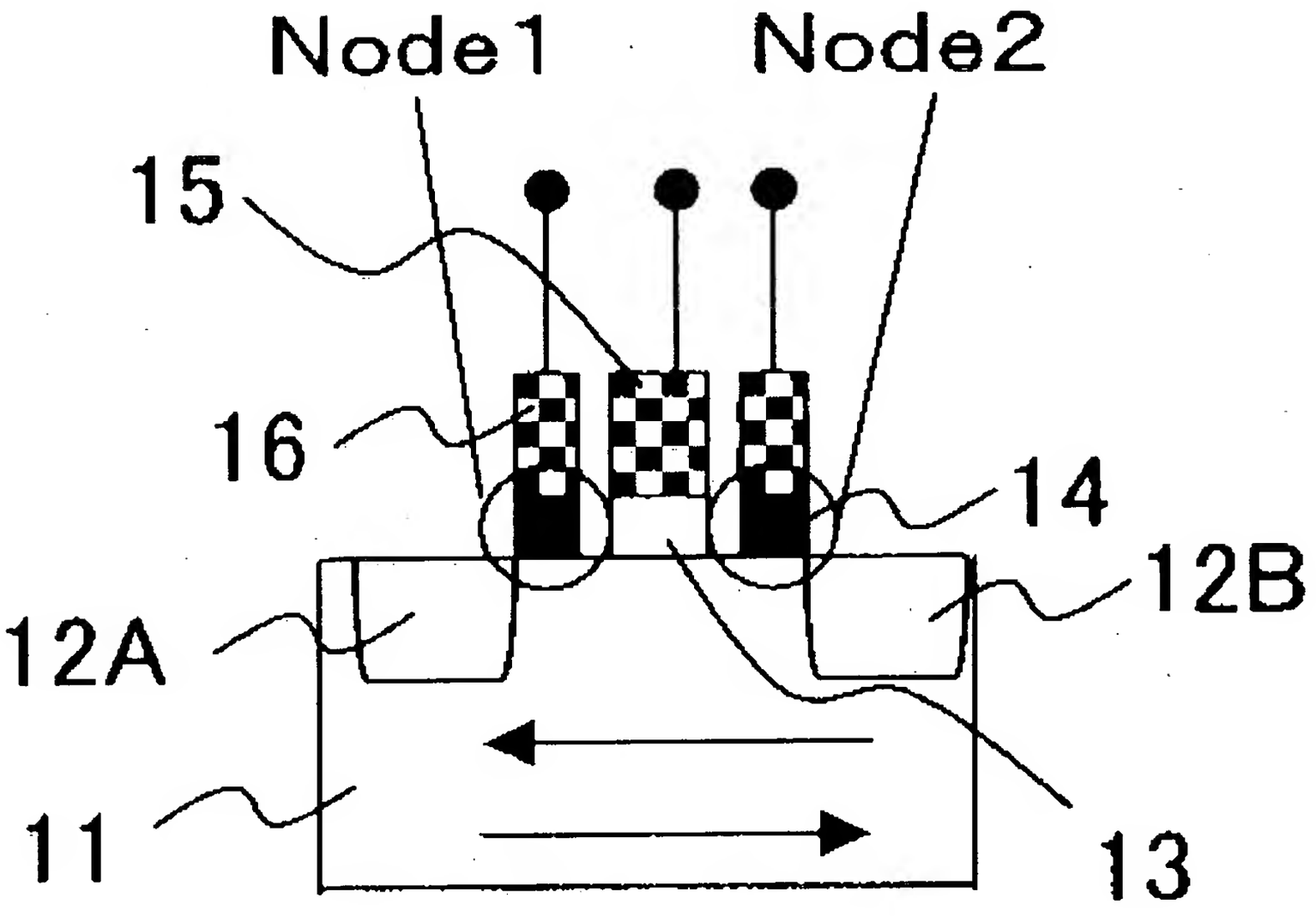


FIG . 24 PRIOR ART

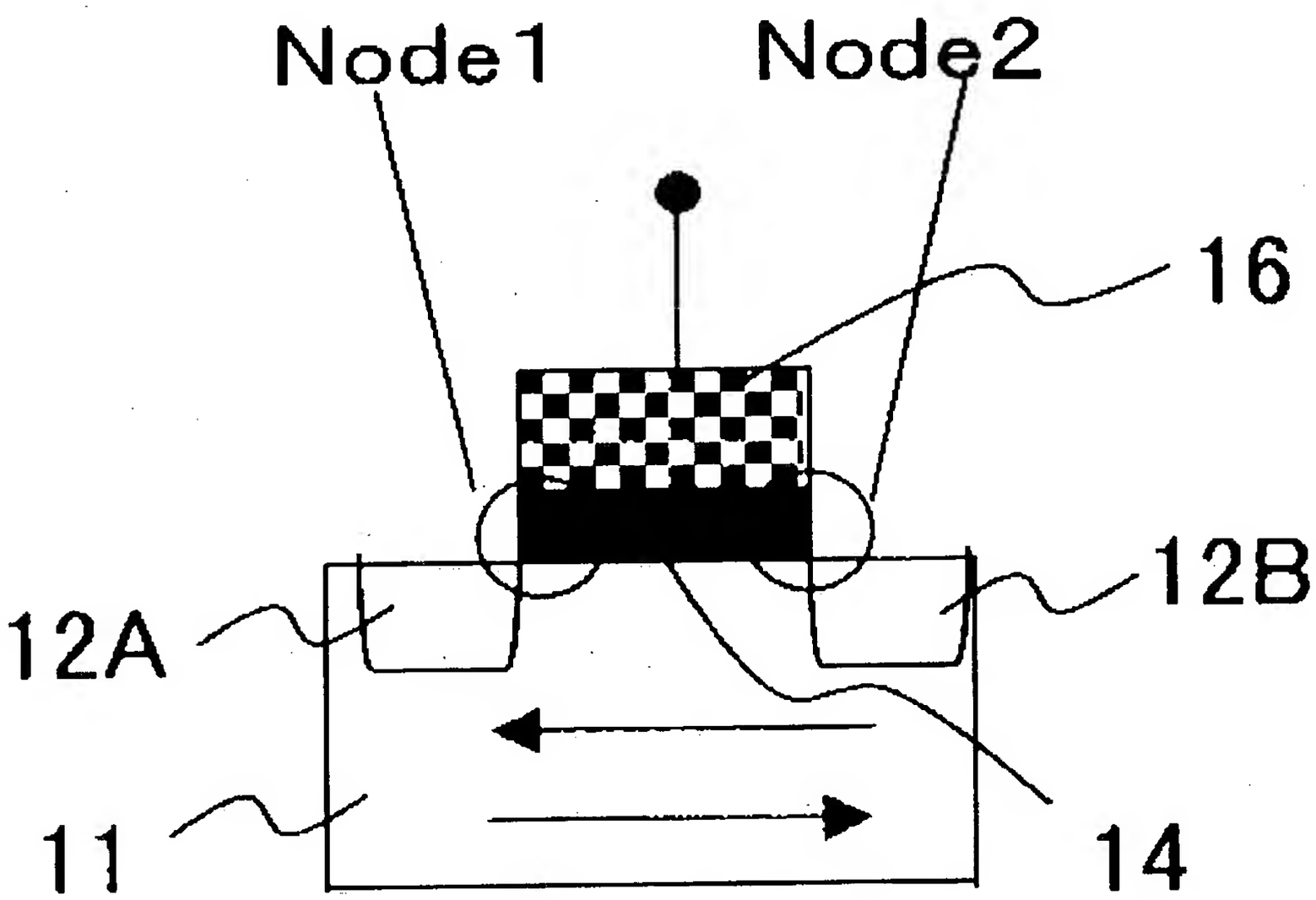


FIG . 25A PRIOR ART

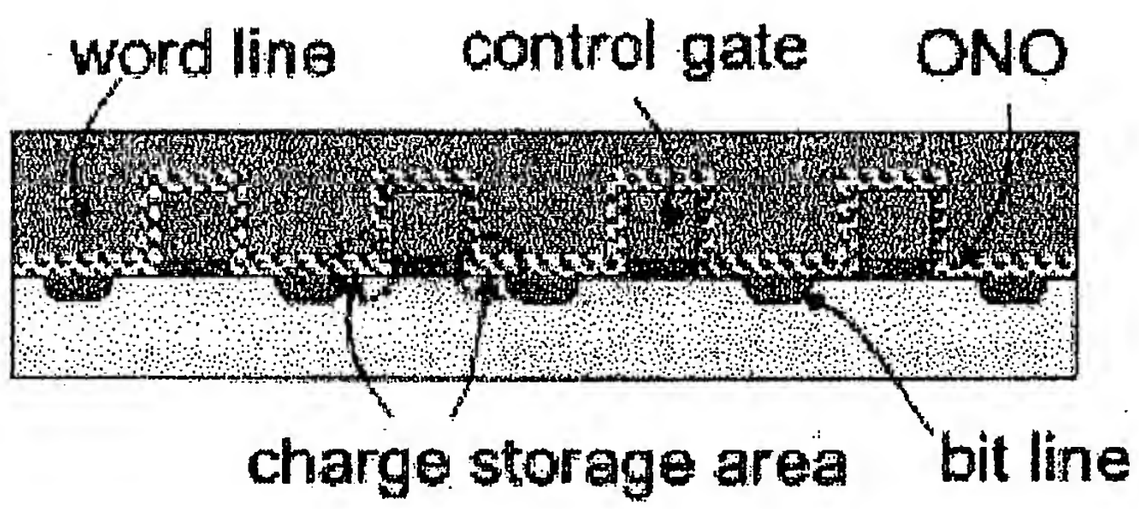


FIG . 25B PRIOR ART

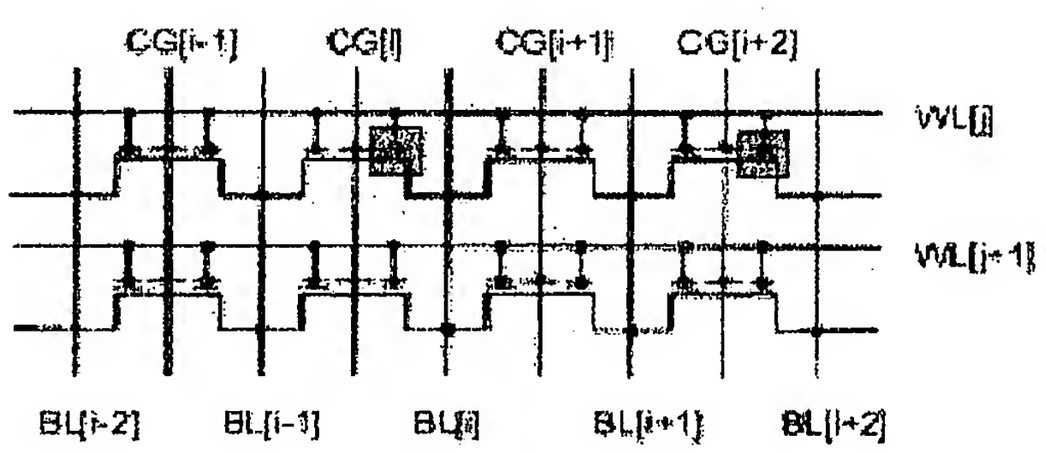


FIG . 25C PRIOR ART

	Wli (j)	WL(k≠j)	BL(I+2n)	BL(I+2n-1)	CG(I+2n)	CG(I+2n-1)
Prog	9.0V	0.0V	5.0V	0.0V	1.0V/0.0V	0.0V
Erase	0.0V	0.0V	7.0V	0.0V	5.0V	0.0V
Read	Vread	0.0V	0.0V	1.5V	1.5V	0.0V

FIG . 26A

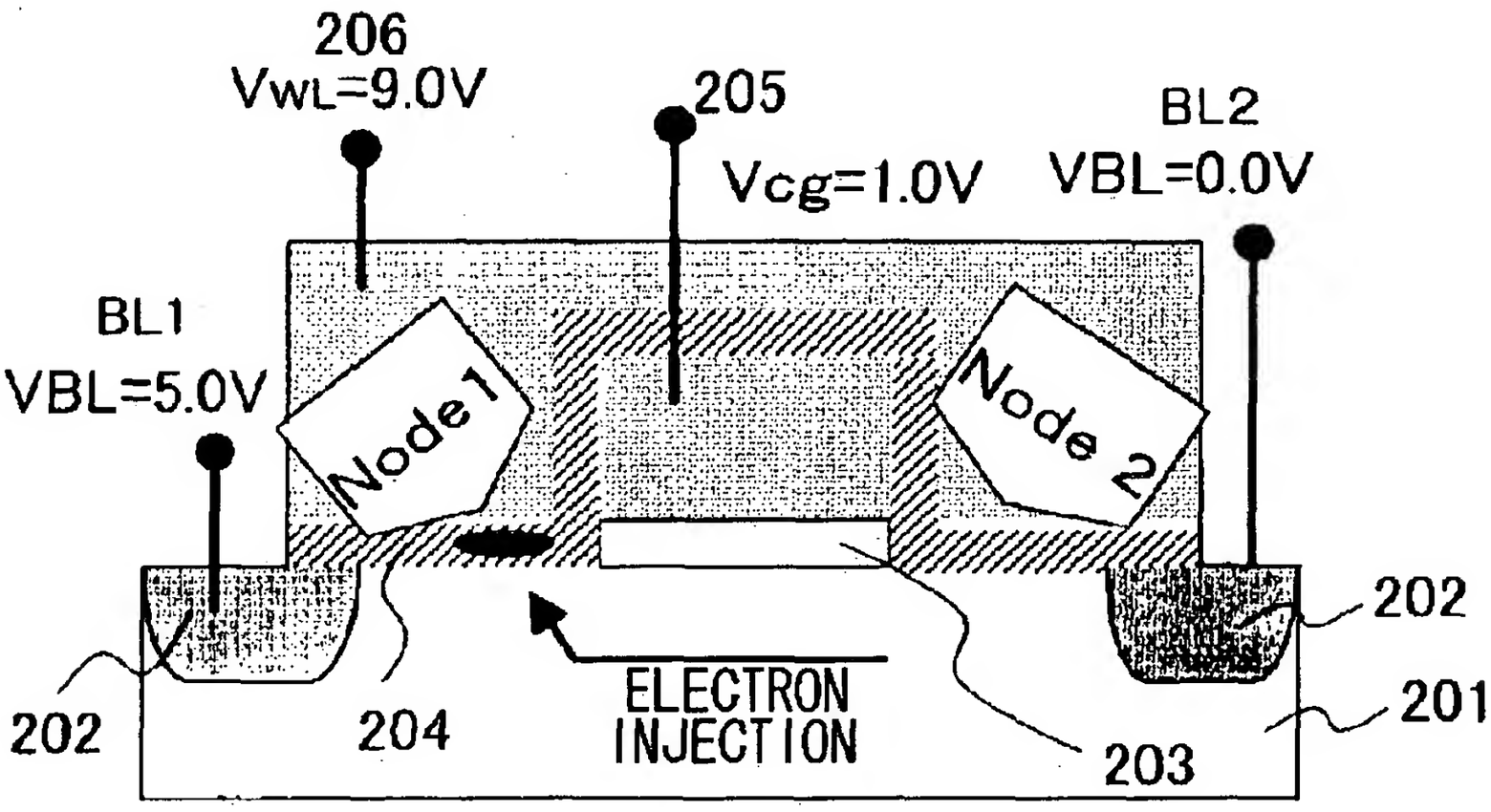


FIG . 26B

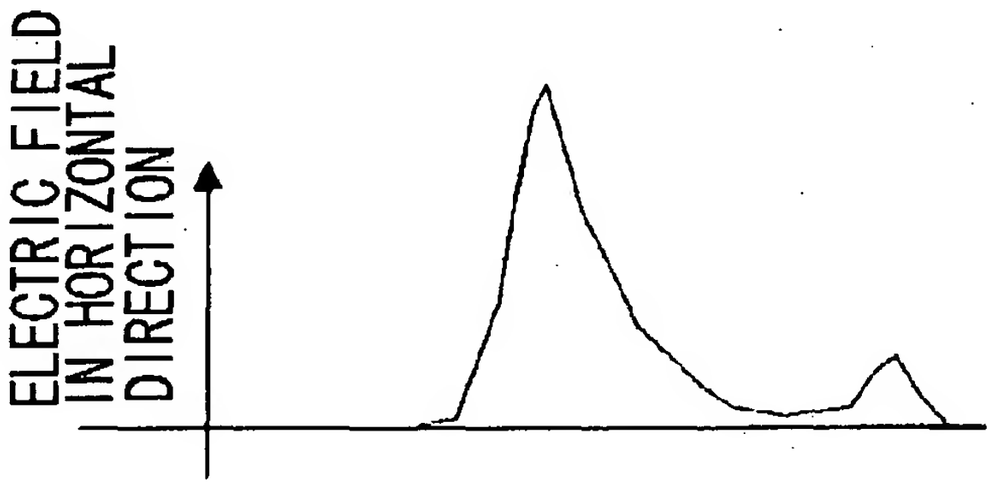


FIG . 27

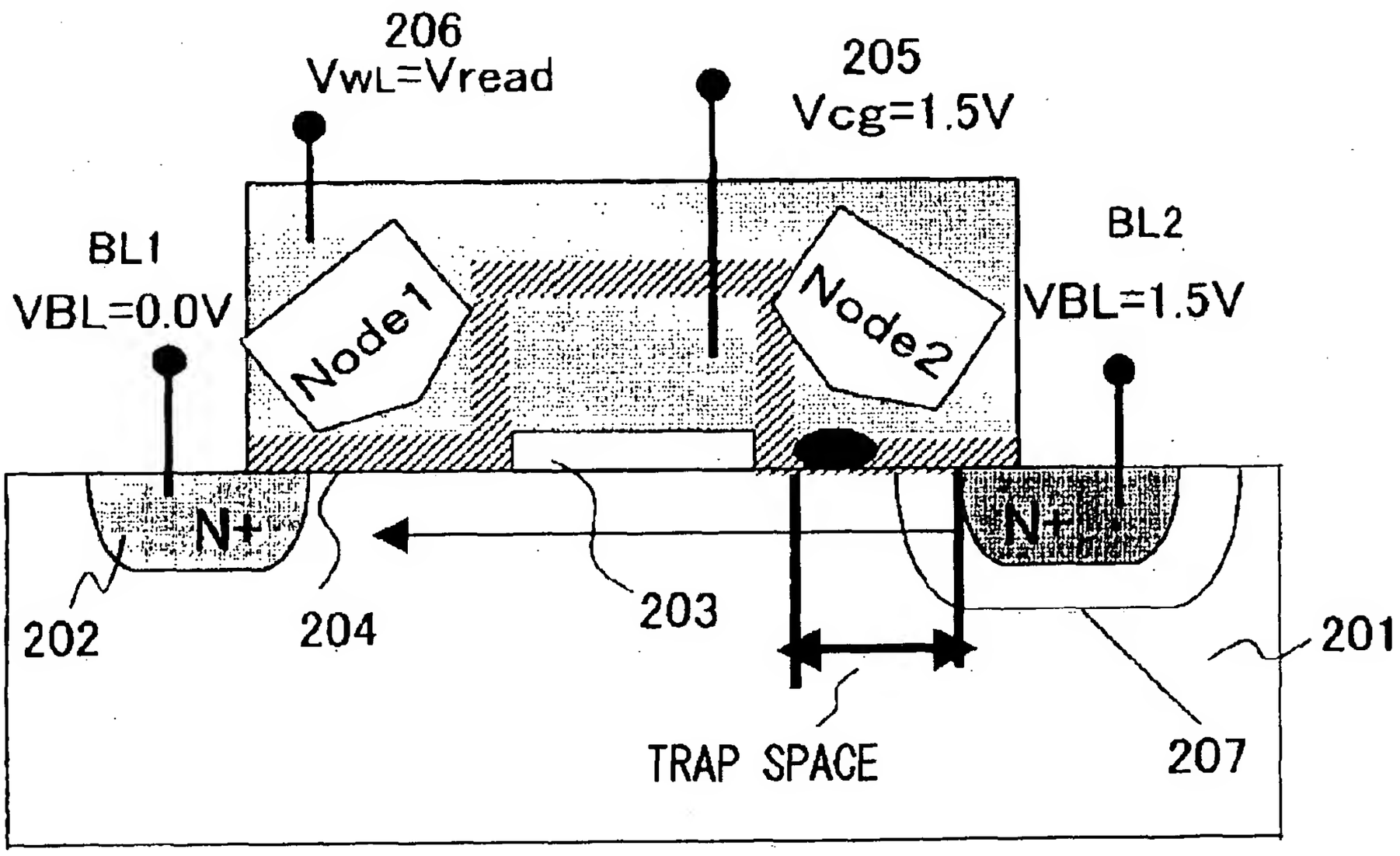
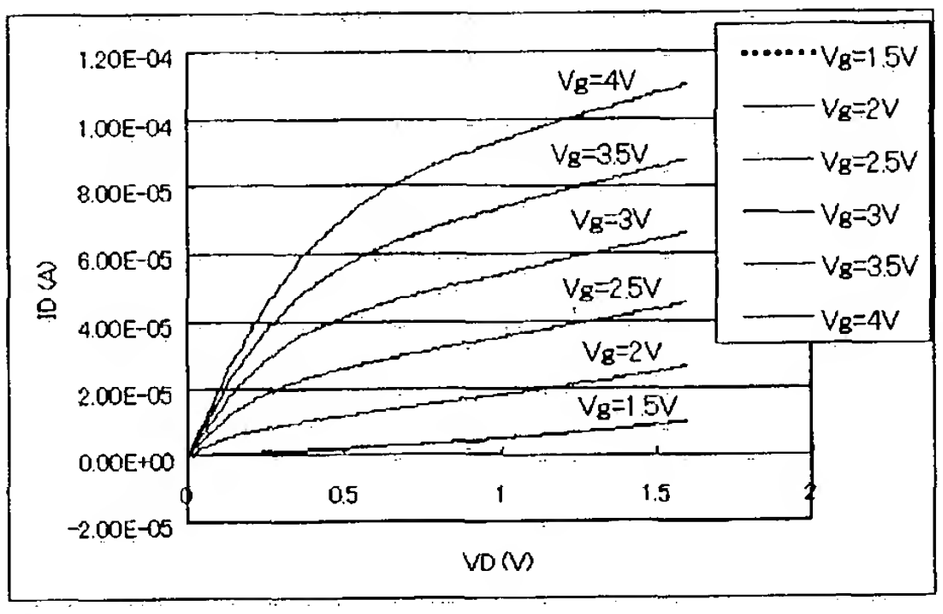
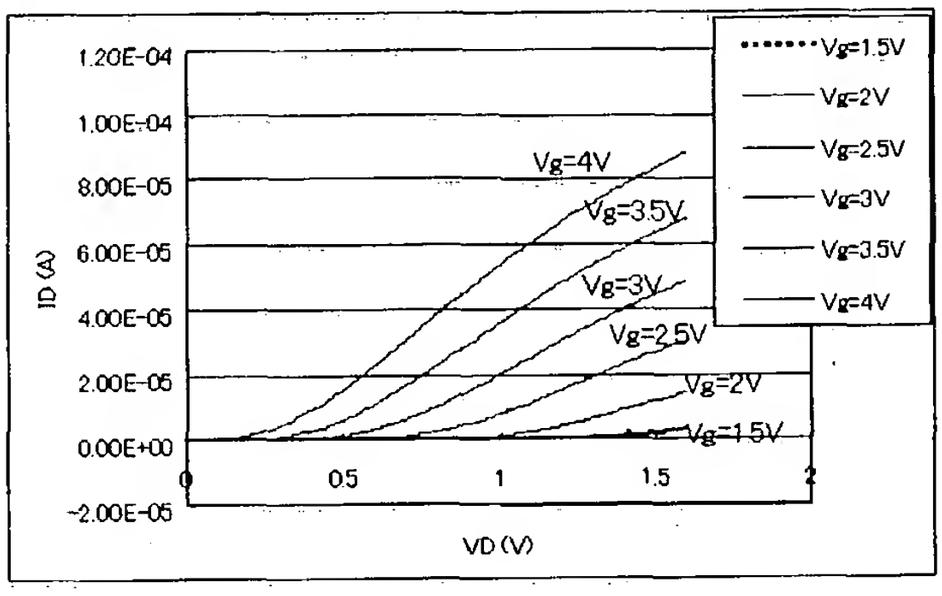

206
VwL=Vread
205
Vcg=1.5V
BL1
VBL=0.0V
Node1
Node2
BL2
VBL=1.5V
N+
N+
202
204
203
201
TRAP SPACE
207

FIG . 28A



Node1:Erased
Node2:Erased

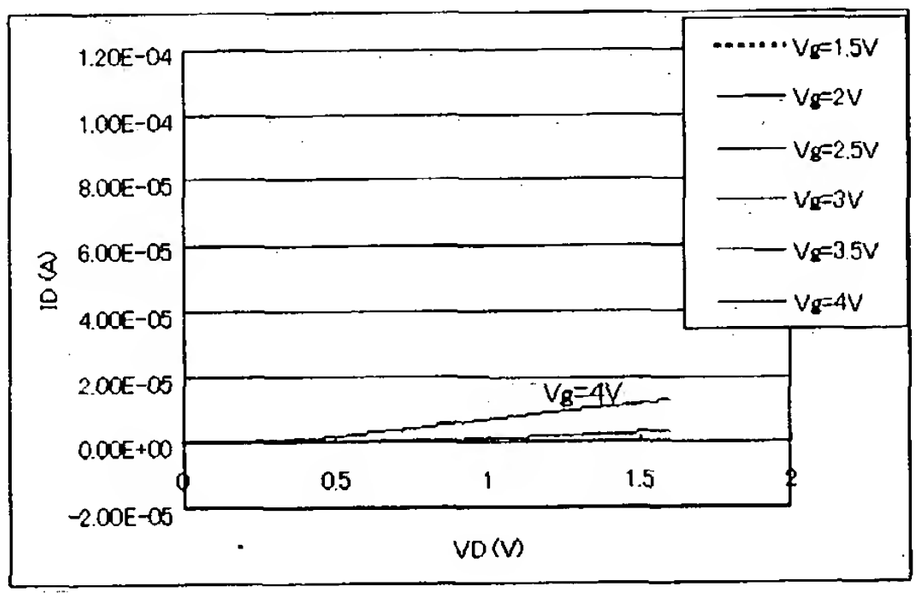
FIG . 28B



Node1:Erased
Node2:Programmed

TRAP SPACE
0.03～0.05um

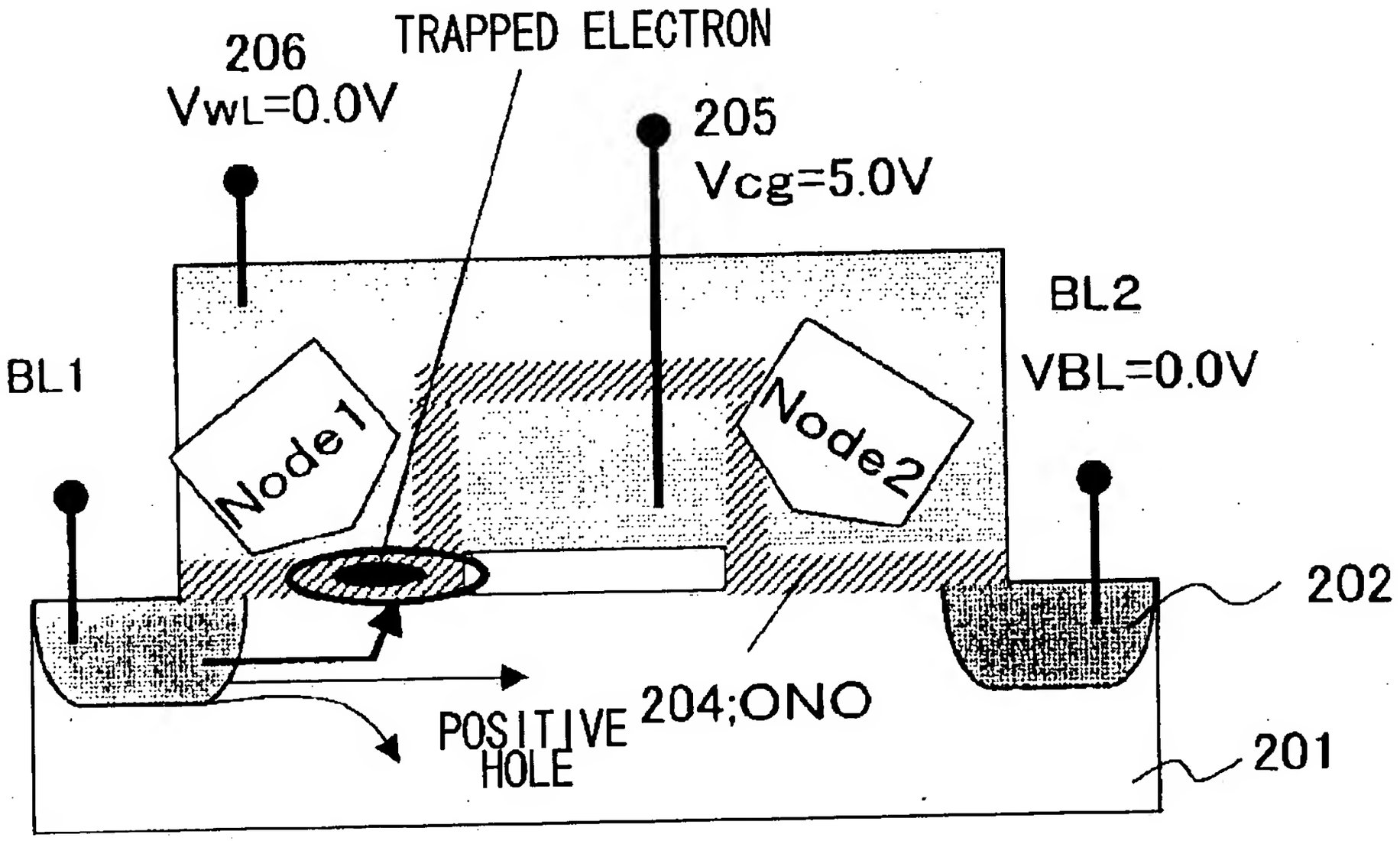
FIG . 28C



Node1:Erased
Node2:Programmed

TRAP SPACE
0.2～0.25um

FIG . 29


206
VWL=0.0V
TRAPPED ELECTRON
205
Vcg=5.0V
BL2
VBL=0.0V
BL1
Node1
Node2
202
204;ONO
POSITIVE
HOLE
201